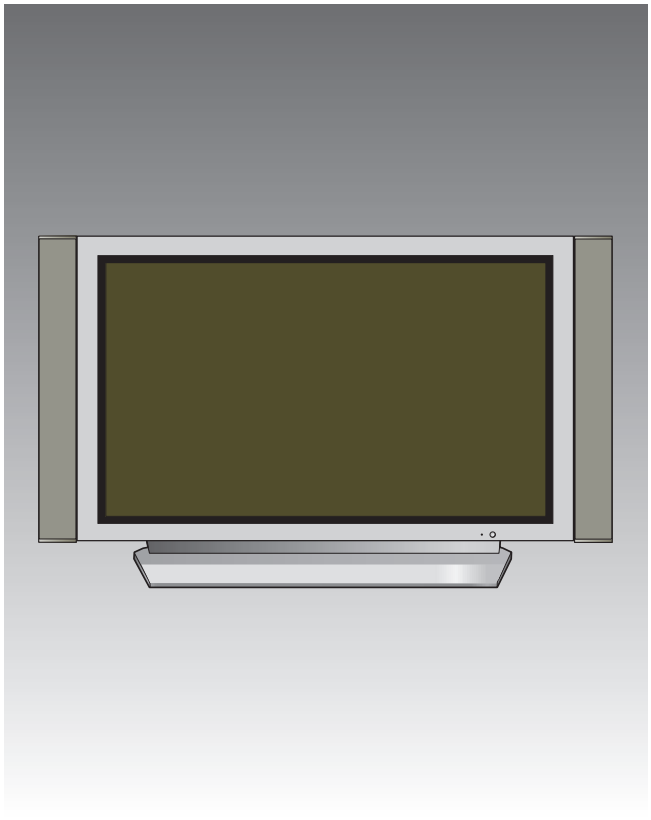
PLASMA DISPLAY TV

Chassis : D54B(N)
Model : PDP4298EDX/SMS (PDP4298ED)

SERVICE Manual

PLASMA DISPLAY TV



CONTENTS

ELECTRONICS

Printed in Korea
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1. Specifications

Model	PL42P3S	SPN4235	PDP4294LV	PDP4298ED
Dimensions	1027 (W) X 79 (D) X 630.5 (H) mm ; 40.43 (W) X 3.11 (D) X 24.82(H) inches			
Weight	31 kg ; 68.34 lbs {37.6 kg ; 82.89 lbs (with stand)}			
Vlotage	100~240V~, 60Hz	120V, 60Hz	120V, 60Hz	120V, 60Hz
Power Consumption	370 Watts	330 Watts	370 Watts	370 Watts
Number of Pixels	852(H) x 480(V)			
Screen Size	107 Cm/42 inches			
ANTENNA input	VHF, UHF (75Ω unbalanced)			
VIDEO input	VIDEO S-VIDEO COMPONENT 1 - 480i / 480p / 720p / 1080i COMPONENT 2 - 480i / 480p / 720p / 1080i RGB : D-SUB 15P DVI			
AUDIO input	VIDEO / S-VIDEO COMPONENT 1 COMPONENT 2 PC (RGB) DVI			
AUDIO output	10W + 10W (8 Ω) Subwoofer (500mv RMS at 1KHz)			

MEMO

2. Alignment and Adjustments

2-1 Service Mode

2-1-1 SERVICE MODE Entry Method (General Transmitter)

■ For the General Transmitter

1. Turn the power off and set to stand-by mode.
2. Press the buttons of the transmitter in this order; Mute-1-8-2-Power to turn the set on.
3. The set turns on and enters service mode.

* If you fail to enter service mode, repeat steps 1 and 2 above.

2-1-2 Initial DISPLAY State of SERVICE MODE

2-1-2(A) OSD DISPLAY

SERVICE MAIN

1. UPD64083	:	COMB-FILTER
2. VPC3230(M)	:	MAIN VCD
3. VPC3230(S)	:	SUB VCD
4. FLI2200	:	DEINTERLACER
5. ASI500 I	:	SCALER MAIN / OSD
6. ASI500 II	:	SCALER PIP
7. DNIe	:	PICTURE ENHANCER
8. CXA2151HD	:	COMPONENT MUX
9. AD9883	:	A/D CONVERTER
10.LOGIC	:	PDP DRIVER
11.TP LOG-ASI	:	TEST PATTERN
12.OPTION		TM_ALS42N02_001
13. RESET		02-12-10 09H

2-1-2(B) Button Operations in SERVICE MODE

Menu	Displays all menus
Joystick UP / DOWN	Cursor move to select items
Joystick (LEFT / RIGHT)	Enable to increase and decrease the data of the selected items

2-1-3 Factory Data by Mode

2-1-3(A) UPD64083 : TV-AV

ITEM	TV/VIdeo/S-Video/Component1,2(SD)	Component1,2(HD)	PC	DVI
VAPGAIN	4	4	4	4
VAPINV	16	16	16	16
YPFP	3	3	3	3
YPFG	9	9	9	9

2-1-3(B) VPC3230 : TV-COMP

ITEM	TV/VIdeo/S-Video/Component1,2(SD)	Component1,2(HD)	PC	DVI
CONTRAST	43	43	43	43
BRIGHTNESS	27	27	27	27
PEAKING	5	5	5	5
CORING	0	0	0	0
LUMA DELAY	255	255	255	255
HPLL SPEED	1	1	1	1
YUV CONTRAST	29	29	29	29
YUV BRIGHTNESS	68	68	68	68
YUV SATCB	42	42	42	42
YUV SATCR	42	42	42	42
YUV TINT	3	3	3	3
SATURATION	2000	2000	2000	2000
TINT	32	32	32	32

2-1-3(C) VPC3230(S) TV COMP

ITEM	TV/VIdeo/S-Video/Component1,2(SD)	Component1,2(HD)	PC	DVI
PIP CONTRAST	43	43	43	43
PIP BRIGHTNESS	27	27	27	27
YUV CONTRAST	29	29	29	29
YUV BRIGHTNESS	68	68	68	68
LUMA DELAY	255	255	255	255
H POSITION	0	0	0	0
V POSITION	0	0	0	0

2-1-3(D) FLI2200 : TV-COMP

ITEM	TV/VIdeo/S-Video/Component1,2(SD)	Component1,2(HD)	PC	DVI
Y CLAMP	0	0	0	0
C CLAMP	512	512	512	512
Y DELAY	4	4	4	4
C DELAY	11	11	11	11
MOTION DETECT	48	48	48	48

2-1-3(E) ASI500 I : ALL (EXCEPT SUB CONT/BRIGHT)

ITEM	TV/VIdeo/S-Video/Component1,2(SD)	Component1,2(HD)	PC	DVI
R CONTRAST	32	32	32	32
G CONTRAST	32	32	32	32
B CONTRAST	32	32	32	32
R BRIGHTNESS	0	0	0	0
G BRIGHTNESS	0	0	0	0
B BRIGHTNESS	0	0	0	0
TEXT ALPHA	1	1	1	1
TEXT THRESHOLD	7	7	7	7
FILTER ML	0	0	0	0
FILTER MR	0	0	0	0
FILTER FR	0	0	0	0
FILTER MC	16	16	16	16
FILTER UC	0	0	0	0
FILTER LC	0	0	0	0
FILTER YPASS	0	0	0	0
R GAMMA	32	32	32	32
G GAMMA	32	32	32	32
B GAMMA	32	32	32	32
H POSITION	0	0	0	0
V POSITION	0	0	0	0
H SIZE	0	0	0	0
V SIZE	0	0	0	0
OVERSCAN B	63	63	63	63
OVERSCAN G	63	63	63	63
OVERSCAN R	63	63	63	63

2-1-3(F) ASI500 II : ALL

ITEM	TV/VIdeo/S-Video/Component1,2(SD)	Component1,2(HD)	PC	DVI
PIP R CONT	32	32	32	32
PIP G CONT	32	32	32	32
PIP B CONT	32	32	32	32
PIP R BRIGHT	0	0	0	0
PIP G BRIGHT	0	0	0	0
PIP B BRIGHT	0	0	0	0
PIP FILTER LC	0	0	0	0
PIP FILTER ML	0	0	0	0
PIP FILTER MR	0	0	0	0
PIP FILTER UC	0	0	0	0

2-1-3(G) DNIe : ALL (EXCEPT SUB BRIGHT/CONT)

ITEM	TV/VIdeo/S-Video/Component1,2(SD)	Component1,2(HD)	PC	DVI
SUB BRIGHT	0	0	0	0
SUB CONT	0	0	0	0
NR SCALE MAX	52	48	48	48
NR SCALE MIN	18	16	16	16
DE GAIN COR	3	3	3	3
DE GAIN CLIP	60	60	60	60
CE UPPER	240	240	240	240
CE CUTOFF	64	64	64	64
CE GAIN	48	48	48	48
WTE Y THRE	230	230	230	230
WTE C THRE	2	2	2	2
SYNC MODE	1	1	1	1
PATT SEL	0	0	0	0

RED CONPENSA	616	616	616	616
BLUE CONPENSA	616	616	616	616
WTE GAIN	58	58	58	58
RAST VSIZE	1023	1023	1023	1023
RAST HSIZE	895	895	895	895
SHARP OFFSET	0	0	0	0

2-1-3(H) CXA2151HD : COMP-PC

ITEM	TV/VIdeo/S-Video/Component1,2(SD)	Component1,2(HD)	PC	DVI
GAIN-SEL	1	1	1	1
CR GAIN	7	7	7	7
CB GAIN	7	7	7	7
YG GAIN	1	1	1	1

2-1-3(I) AD9883 : COMP-PC

ITEM	TV/VIdeo/S-Video/Component1,2(SD)	Component1,2(HD)	PC	DVI
R GAIN	142	142	142	142
G GAIN	142	142	142	142
B GAIN	142	142	142	142
R, CR OFFSET	60	60	54	54
G, Y OFFSET	48	48	54	54
B, CB OFFSET	64	64	54	54
AUTO COLOR	-	-	-	-

AUTO COLOR : Automatic white balance adjustment in pc mode and component(HD) mode.

2-1-3(J) LOGIC : ALL (EXCEPT DRIVE/CUTOFF)

ITEM	TV/VIdeo/S-Video/Component1,2(SD)	Component1,2(HD)	PC	DVI
R DRIVE	140	140	140	140
G DRIVE	130	130	130	130
B DRIVE	120	120	120	120
R CUTOFF	0	0	0	0
G CUTOFF	0	0	0	0
B CUTOFF	0	0	0	0
GAMMA	1	1	1	1
GTS SET	0	0	0	0
ERD MODE	2	2	2	2
RANDOM NOISE	0	0	0	0
DIFF FILTER	1	1	1	1
APC	1	1	1	1
APC SET	0	0	0	0
APC VALUE	127	127	127	127
ACTIVE VPOS	12	12	12	12
ACTIVE HPOS	19	19	19	19
VSYNC POS	3	3	3	3
HSYNC POS	32	32	32	32
VSYNC WIDTH	2	2	2	2
HSYNC WIDTH	12	12	12	12

2-1-3(K) TP LOG-ASI : ALL

ITEM	TV/VIdeo/S-Video/Component1,2(SD)	Component1,2(HD)	PC	DVI
LOG PATTERN	0	0	0	0
LOG HIGH LEVEL	255	255	255	255
LOG LOW LEVEL	0	0	0	0
ASI COLOR BAR	0	0	0	0

2-1-3(L) OPTION : ALL

ITEM	TV/VIdeo/S-Video/ Component1,2(SD)	Component1,2(HD)	PC	DVI	Adjustment
PIX SHIFT	0	0	0	0	0:OFF 1:RF,Video,S-Video,Component1,2 2:PC 3:ALL
SHIFT TEST	0	0	0	0	0:minute 1:second
PIX NUMBER	1	1	1	1	Number of pixels that shift left/right
SHIFT LINE	1	1	1	1	Number of lines that shift up/down
SHIFT TIME	4	4	4	4	Time set during shift test
NUMBER RANGE	4	4	4	4	Shift range
LINE RANGE	4	4	4	4	Shift range
COUNTRY	0	0	0	0	0:Korean 1:America 2:Japan
TEMP PROTECT	0	0	0	0	Not used
DNIe DEMO	0	0	0	0	0:OFF 1:ON
DNIe THROUGH	0	0	0	0	0:Not through 1:Through
VIDEO MUTE	10	10	10	10	Unit:100mese
IRC AFN	0	0	0	0	0:General American mode 1:Military American mode
LANGUAGE	0	0	0	0	0:English 1:French 2:Spanish
CUSTOMER	0	0	0	0	0:CE 1:VMB
TUNER	1	1	1	1	0:1 TUNER 1:2 TUNER
PILOT HIGH	21	21	21	21	Stereo ↔ mono boundary value
PILOT LOW	16	16	16	16	Stereo ↔ mono boundary value
RESET	-	-	-	-	Customer settings reset

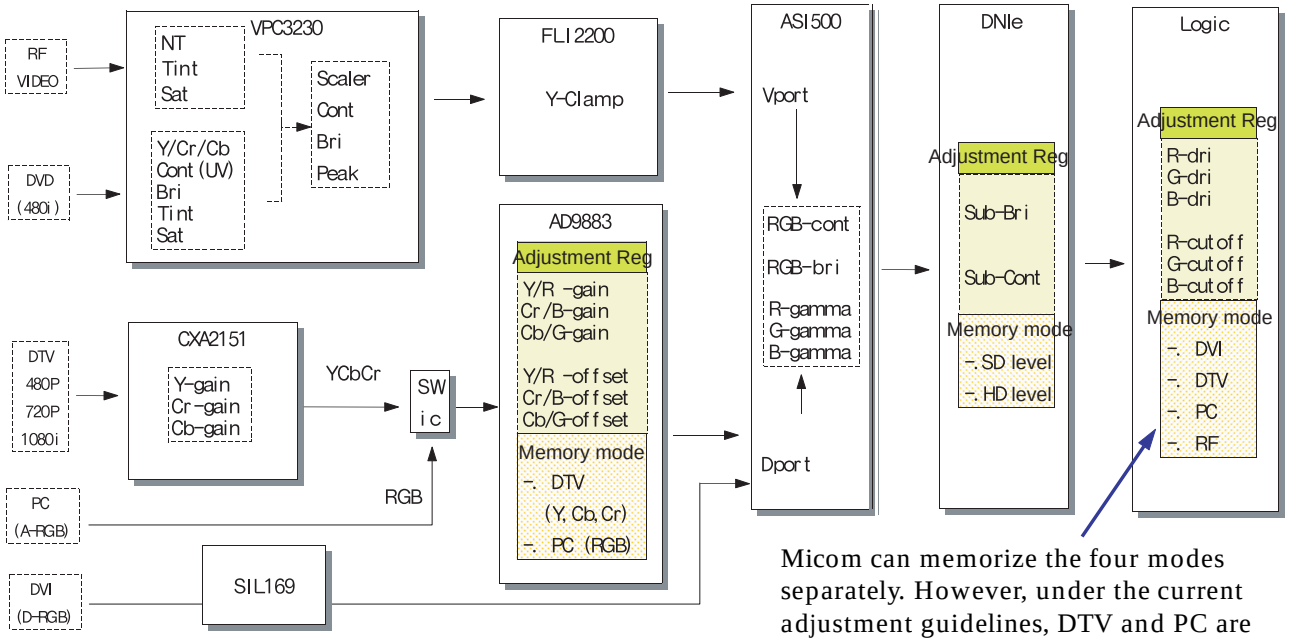
Alignment and Adjustments

2-2 WHITE Balance Coordinates

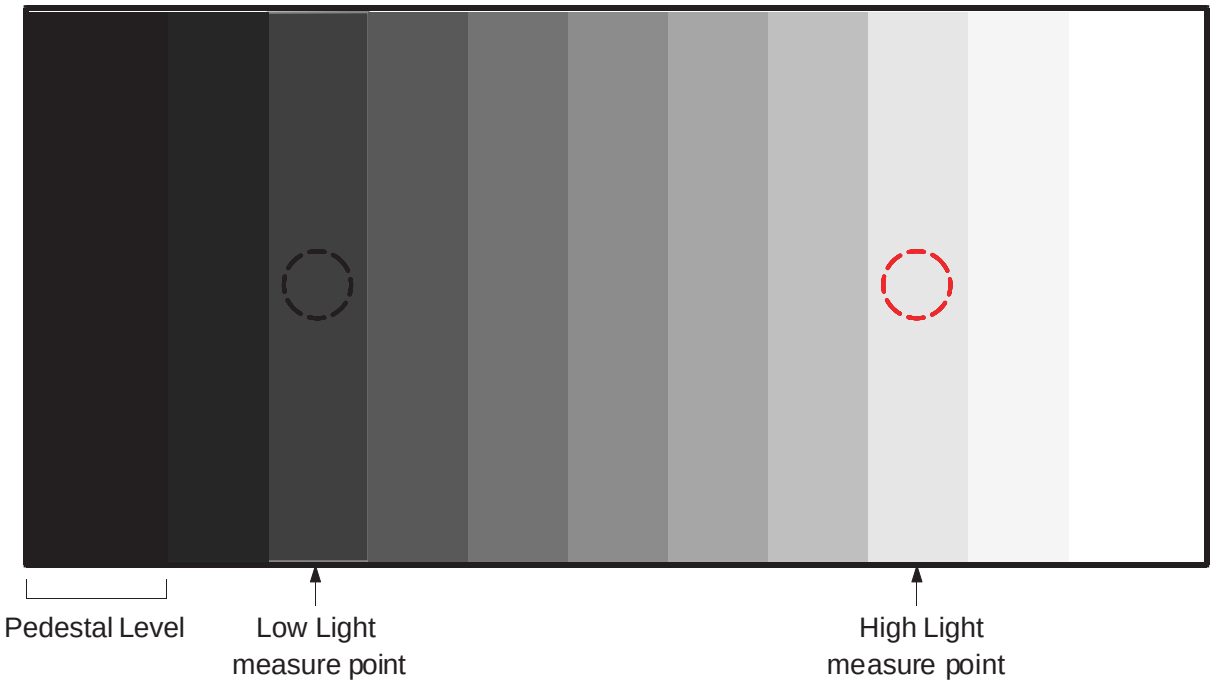
2-2-1 SPN4235 White Balance Adjustment

1. W/B Adjustment is required for the following four modes: DVI → DTV → PC → RF
2. Adjustment Method (DVI, DTV, PC : VG828, RF : Adjust RF signals to match the Toshiba pattern (in-house signal)
   - ① Adjust the target set by adjusting the panel logic and the video DNIe adjustment register in register in order to determine the referential W/B of the panel with a DVI input, which is the full digital path.
   - ② For DTV adjustment, adjust the adjustment register of AD9883 to align the DTV signal to the DNIe and logic panel value which was fixed with a DVI adjustment so that they are in effect considered to be the same signals. (At this time, do not adjust the gain of AD9883 → the Highlight W/B does not need to be adjusted since its deviation falls within valid distribution range.)
   - ③ PC adjustment is same as DTV adjustment. (The offset can be applied to the values obtained through DTV adjustment. However, additional adjustment is required for Y, Cb, and Cr of DTV since PC processes R, G, and B signals.)
   - ④ RF adjustment is performed with the Toshiba pattern (in-house signal) and differs from the VG828 signals in the above three modes. Hence, it should be performed with the same method of ① DVI adjustment.

※ Thus, Micom saves the W/B data separately for each memory mode of the block (See the block diagram given below) during W/B adjustment.



2-2-2 White Balance Coordinates by Mode



		DVI	DTV COMPONENT (480P, 720P, 1080i)	PC	VIDEO
H/L	x	285	285	290	285
	y	290	290	305	300
	Y(fL)	32.0	33.0	17.6	33.0
L/L	x	285	285	290	285
	y	295	290	300	295
	Y(fL)	1.3	1.2	1.0	1.4

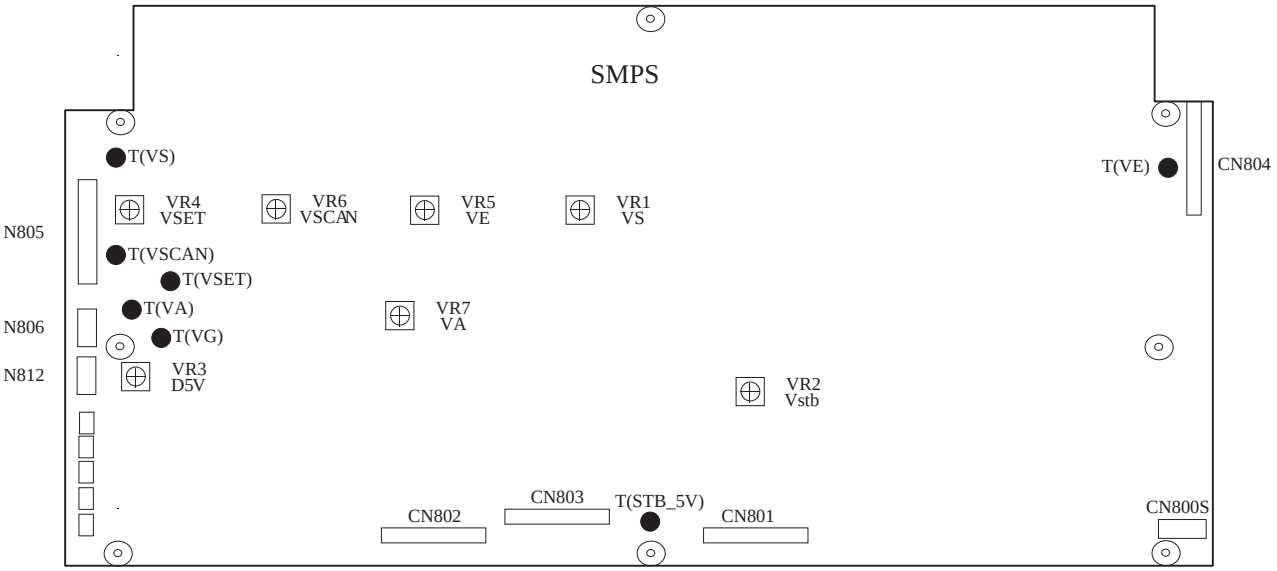
= Pattern Used in Adjustment : 10 Steps Gray scale pattern

2-3 Voltage Adjustment

● Turning the variable resistor(VR) adjusts voltage.

T : Test Point

⊕ VR: Variable Resistor



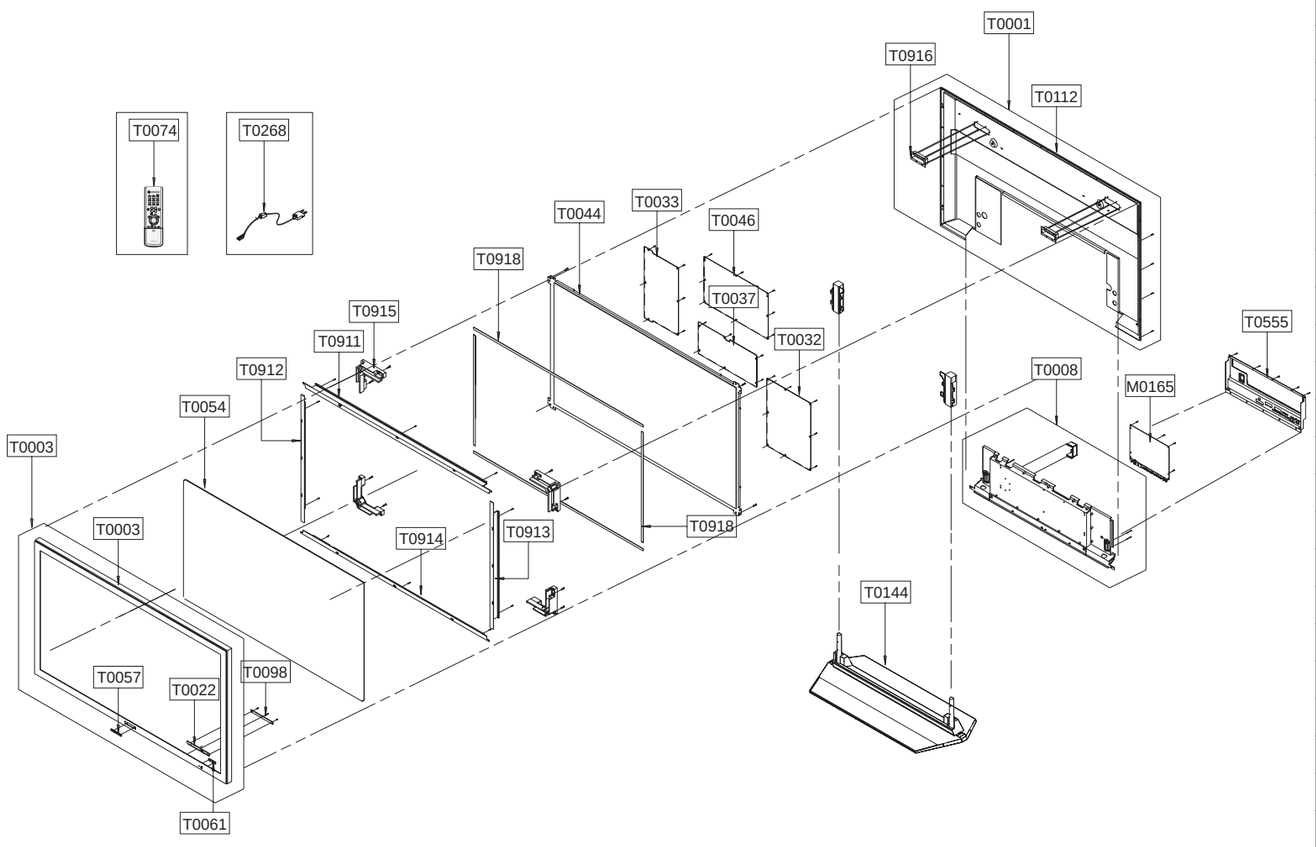
OUTPUT	Voltage(V)
VA	See the labels attached on the base chassis.
VSCAN(VSC)	
VS	
VE	
VSET	
D5V	+5V
STB_5V	+5V
VG	+15V

MEMO

3. Exploded View & Parts List

3-1 PDP4298EDX/SMS

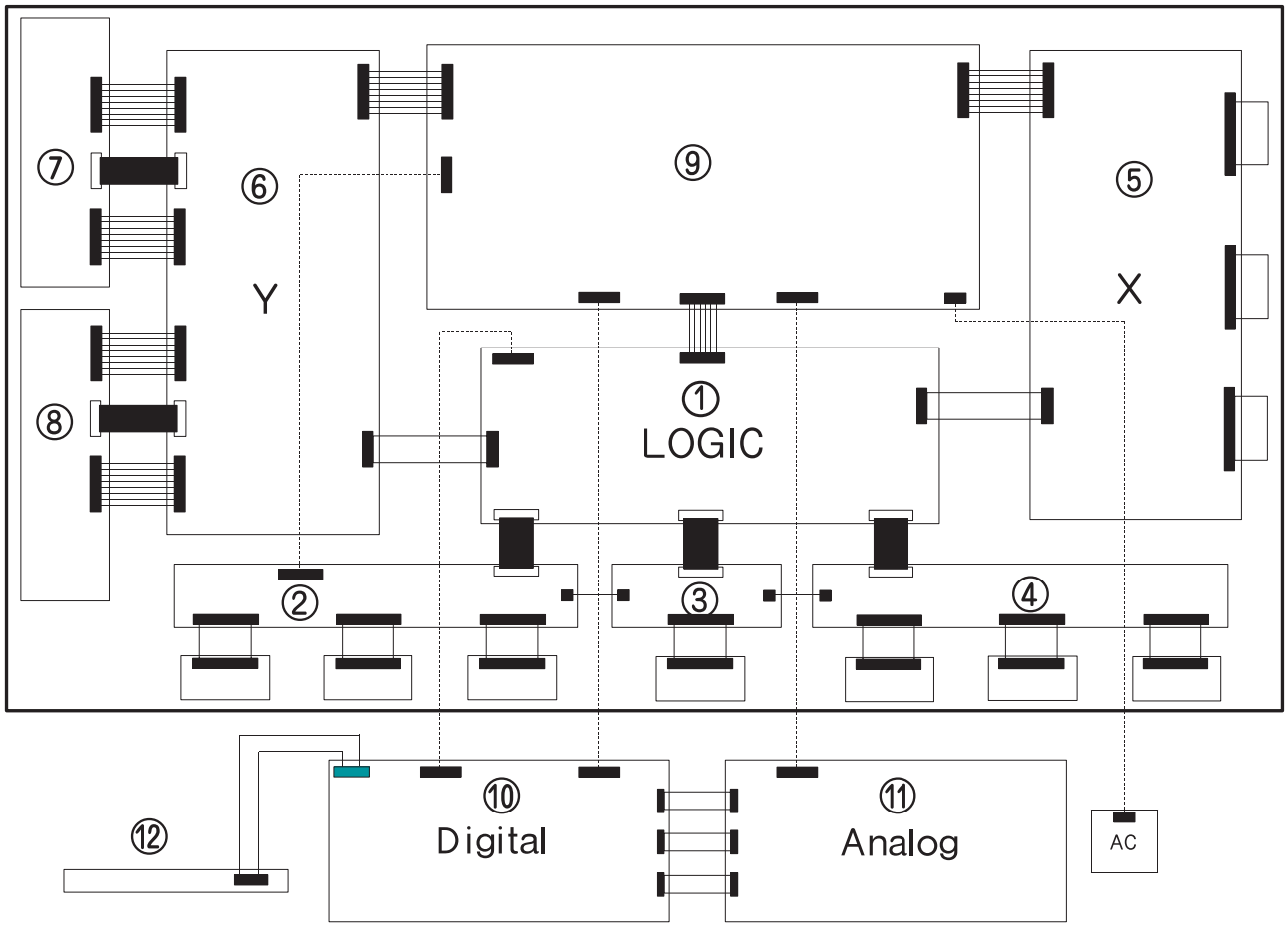
Yon can search for the updated part code through ITSELF web site.
URL:http://itself.sec.samsung.co.kr



Loc.No.	Code No.	Description;Specification	Q'ty	S.N.A
M0165	BN94-00494E	ASSY PCB MISC-2 TUNER DIGITAL;PDP4294X/S	1	
T0001	BN96-00314A	ASSY COVER P-BACK;42P3H,AL 5052,T1.2	1	
T0003	BN96-00737C	ASSY COVER P-FRONT;PDP4298,AKAI,HIPS V0,	1	
T0003	BN64-00206A	CABINET FRONT;PDP4294,HIPS V0,GRAY	1	S.N.A
T0008	BN96-00313B	ASSY COVER P-BACK SUB;PS42P3S,AL5052 T1.	1	S.N.A
T0022	BP64-00045D	KNOB-CONTROL;PDP4294,ABS,HB,SV-704P,AKAI	1	S.N.A
T0032	BN96-00257A	ASSY PDP P-PBA,Y MAIN;LJ92-00636A,SPD-42	1	
T0033	BN96-00256A	ASSY PDP P-PBA,X MAIN;LJ92-00635A,SPD-42	1	
T0037	BN96-00710A	ASSY PDP P-PBA,L MAIN;M3,S42SD-YD04,42SD	1	
T0044	BN96-00709A	ASSY PDP MODULE P;M3,S42SD-YD03,D54A,S2.	1	
T0046	BN96-00249A	ASSY PDP P-SMPS;,42P3S/50P3H,42SD/50HD,4	1	
T0054	BN64-00122A	SCREEN-EMI,FILTER;FILTER,42P3,984*584,T3	1	
T0057	AA64-03228A	BADGE-BRAND;54J7,AL,T1.5,12,51.2,BLACK,A	1	S.N.A
T0061	BN64-00074B	WINDOW-REMOTE;42P3S,PMMA,,,,,,CLEAR	1	S.N.A
T0074	BN59-00347C	REMOCON;TM63,ALEXANDER,47,SVM-3012,DO	1	
T0098	BN94-00494B	ASS'Y PCB MISC-CONTROL;SPN4235,D54B,ALEX	1	
T0112	BN63-00529A	COVER-BACK;42P3H,AL 3031,T1.2,DGM-5810	1	S.N.A
T0144	BN96-00137B	ASSY COVER P-STAND BASE;PDP-4295ED,AKAI,	1	
T0268	3903-000085	CBF-POWER CORD;DT,US,BP3/YES,I(IEC C13/C	1	
T0555	BN96-00286C	ASSY MISC P-BRACKET TERMINAL;P3,U.S.A	1	S.N.A
T0911	BN61-00244H	BRACKET-FILTER TOP ASSY;42P3S,AL5052,T1.	1	S.N.A
T0912	BN61-00245H	BRACKET-FILTER SIDE L;42P3S,AL5052,1.2	1	S.N.A
T0913	BN61-00309E	BRACKET-FILTER SIDE R;42P3S,AL5052,1.2	1	S.N.A
T0914	BN61-00246G	BRACKET-FILTER BOTTOM ASSY;42P3S,AL5052,	1	S.N.A
T0915	BN61-00141A	HOLDER-MODULE;42P3,AL,DIECASTING	4	S.N.A
T0916	BN61-00202A	BRACKET-HANDLE;42P3S,AL5052,T1.5,DGM-S81	2	S.N.A
T0918	AA60-00110G	SPACER-FILTER;42P3,P/U FROM,560,5,6	1	S.N.A
T0918	AA60-00110J	SPACER-FILTER;50P3,P/U Form,20.0,2.0,5.0	2	S.N.A

4. Service Item

4-1 Assy Board & Part List for Service



No	Description	Code No	Specification
	ASSY PDP P-MODULE	BN96-00709A	M3,S42SD-YD03,D54A,S2.0,1015 x 613,852 x 480,NTSC/PAL,42",ASIC
①	ASSY PDP P-PBA,L MAIN	BN96-00710A	M3,S42SD-YD04,42SD S2.0,79mm logic board,LJ92-00817A
②	ASSY PDP P-PBA,L BUFF(E)	BN96-00253A	LJ92-00632A,SPD-42P3,D54A,42",ALEXANDER ,SD,SDI CODE
③	ASSY PDP P-PBA,L BUFF(F)	BN96-00254A	LJ92-00633A,SPD-42P3,D54A,42",ALEXANDER ,SD,SDI CODE
④	ASSY PDP P-PBA,L BUFF(G)	BN96-00255A	LJ92-00634A,SPD-42P3,D54A,42",ALEXANDER ,SD,SDI CODE
⑤	ASSY PDP P-PBA,X MAIN	BN96-00256A	LJ92-00635A,SPD-42P3,D54A,42",ALEXANDER ,SD,SDI COD
⑥	ASSY PDP P-PBA,Y MAIN	BN96-00257A	LJ92-00636A,SPD-42P3,D54A,42",ALEXANDER ,SD,SDI CODE
⑦	ASSY PDP P-PBA,Y BUFF(UP)	BN96-00258A	LJ92-00637A,SPD-42P3,D54A,42",ALEXANDER ,SD,SDI CODE
⑧	ASSY PDP P-PBA,Y BUFF(DOWN)	BN96-00259A	LJ92-00638A,SPD-42P3,D54A,42",ALEXANDER ,SD,SDI CODE
⑨	ASSY PDP P-SMPS	BN96-00249A	42P3S/50P3H,42SD/50HD,445*245,42MM_MAX,90V~264V,NTSC/PAL,SEMCO
⑩	ASSY PCB MISC-2 TUNER DIGITAL	BN94-00494E	PDP4294X/SMS,D54B,SAMS CLUB
⑪	ASSY PCB MISC-2 TUNER ANALOG	BN94-00421A	SPD-50P3H,D57A
⑫	ASSY PCB MISC-CONTROL	BN94-00494B	SPN4235,D54B,ALEX
	SCREEN-EMI,FILTER	BN64-00122A	FILTER,42P3,984*584,T3.0,0.1ohm,T47%

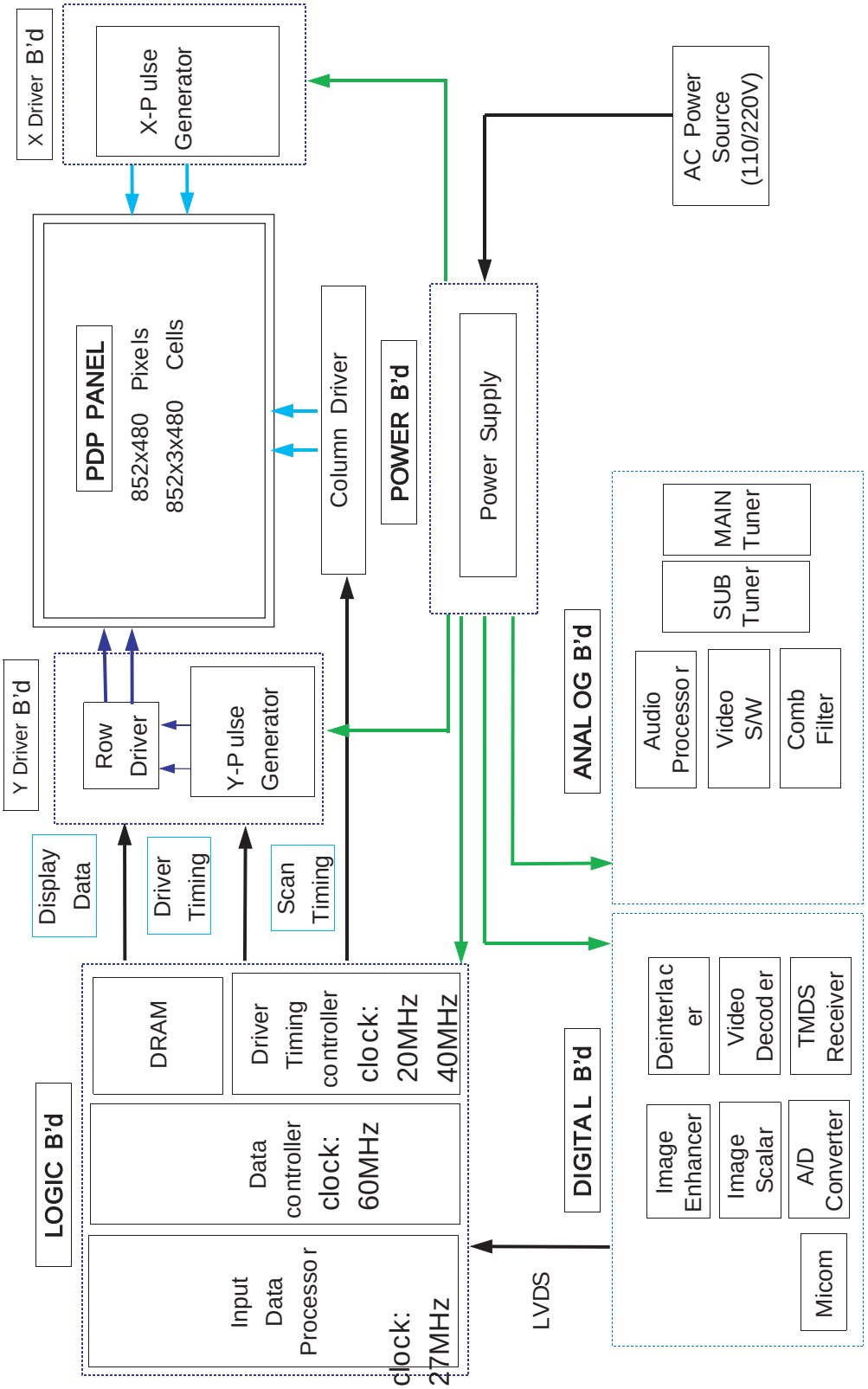
4-2 PDP4298EDX/SMS

Yon can search for the updated part code through ITSELF web site.
URL:http://itself.sec.samsung.co.kr

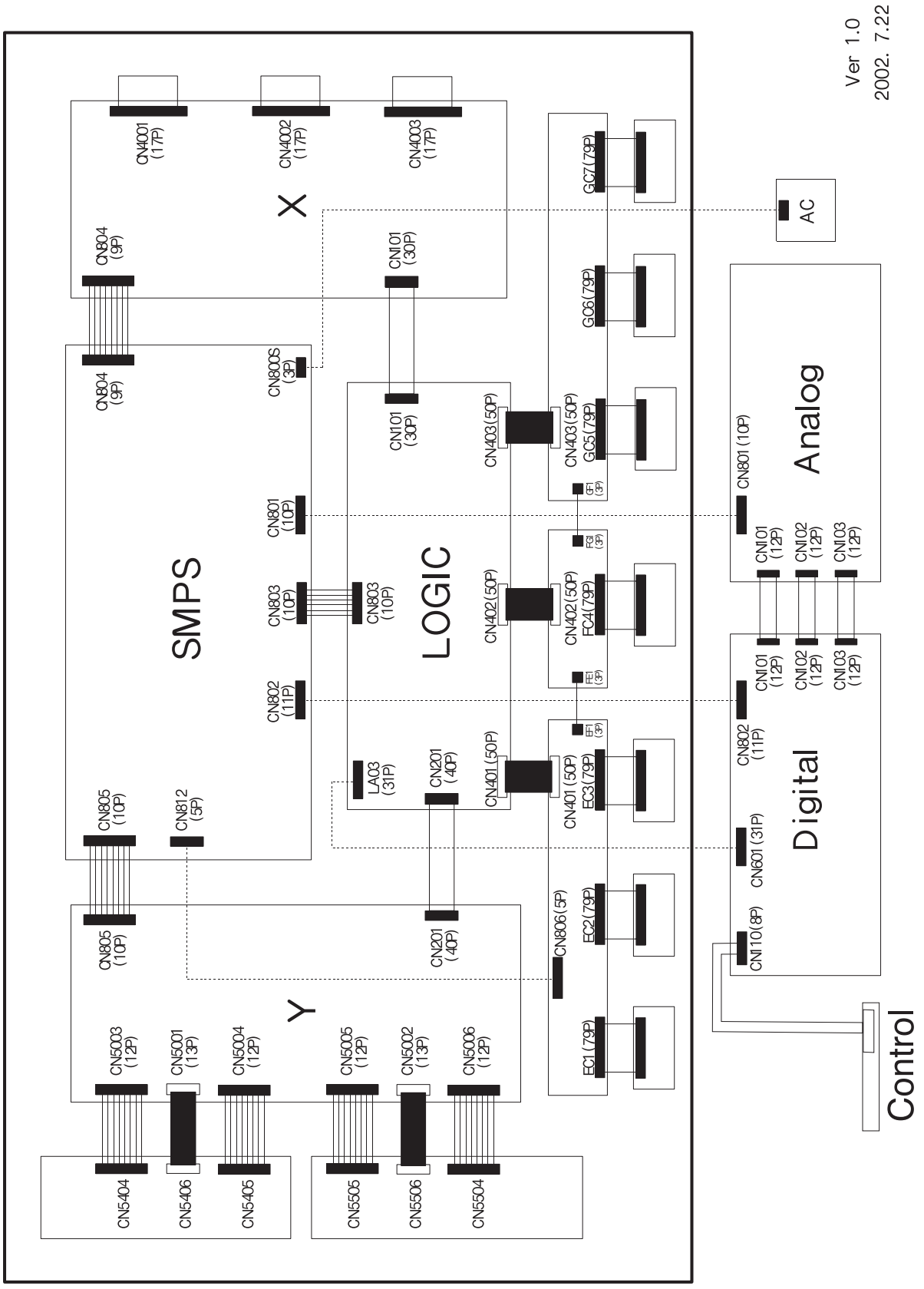
Loc.No.	Code No.	Description;Specification	Q'ty
CIS3	BN40-00007A	TUNER;TCPN9081PC27D,TCPN9081PC27D,45.75M	1
CIS3	BN40-00017A	TUNER;TCLN9081PC27S(S),NTSC,181CH,45.75M	1
M0165	BN94-00494E	ASSY PCB MISC-2 TUNER DIGITAL;PDP4294X/S	1
M0166	BN94-00421A	ASSY PCB MISC-2 TUNER ANALOG;SPD-50P3H,D	1
T0001	BN96-00314A	ASSY COVER P-BACK;42P3H,AL 5052,T1.2	1
T0003	BN96-00737C	ASSY COVER P-FRONT;PDP4298,AKAI,HIPS V0,	1
T0014	BN96-00259A	ASSY PDP P-PBA,Y BUFF(DOWN);LJ92-00638A,	1
T0032	BN96-00257A	ASSY PDP P-PBA,Y MAIN;LJ92-00636A,SPD-42	1
T0033	BN96-00256A	ASSY PDP P-PBA,X MAIN;LJ92-00635A,SPD-42	1
T0037	BN96-00710A	ASSY PDP P-PBA,L MAIN;M3,S42SD-YD04,42SD	1
T0038	BN96-00253A	ASSY PDP P-PBA,L BUFF(E);LJ92-00632A,SPD	1
T0039	BN96-00254A	ASSY PDP P-PBA,L BUFF(F);LJ92-00633A,SPD	1
T0040	BN96-00255A	ASSY PDP P-PBA,L BUFF(G);LJ92-00634A,SPD	1
T0044	BN96-00709A	ASSY PDP MODULE P;M3,S42SD-YD03,D54A,S2.	1
T0046	BN96-00249A	ASSY PDP P-SMPS;,42P3S/50P3H,42SD/50HD,4	1
T0048	BN96-00258A	ASSY PDP P-PBA,Y BUFF(UP);LJ92-00637A,SP	1
T0054	BN64-00122A	SCREEN-EMI,FILTER;FILTER,42P3,984*584,T3	1
T0074	BN59-00347C	REMOCON;TM63,ALEXANDER,47,SVM-3012,DO	1
T0098	BN94-00494B	ASS'Y PCB MISC-CONTROL;SPN4235,D54B,ALEX	1
T0144	BN96-00137B	ASSY COVER P-STAND BASE;PDP-4295ED,AKAI,	1
T0175	BN96-00201D	ASSY SPEAKER P;8ohm,PSN4294,One-packing,	1
T0568	BN39-00338A	CBF IF;D56A/PS42P3S,1P,1365#26,50MM,BLAC	1

5. Circuit Description

5-1 BLOCK DIAGRAM

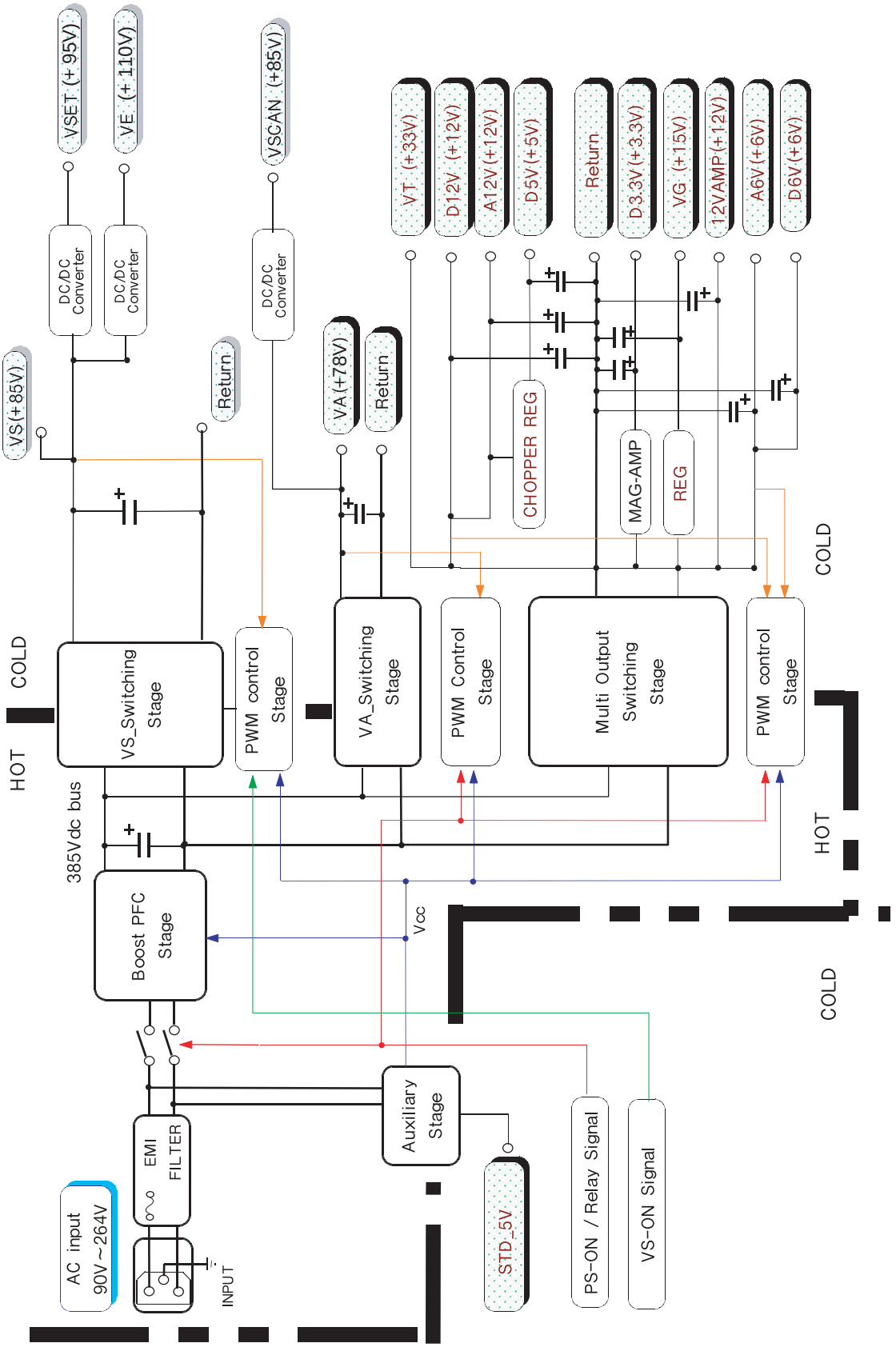


5-2 WIRE DIAGRAM



5-3 POWER SUPPLY

5-3-1 Block Diagram



5-3-2 Circuit Description

1. Outline (PDP42inch SMPS)

Considering various related conditions, the switching regulator with good fficiency and allowing for its small size and light weight was used as the power supply for PDP 50inch (Alexander), VS requiring high power consumption used Asymmetrical Half Bridge converter and flyback converter and other high voltage (VSCAN, VSET, VE) used DC/DC converter. To comply with the international harmonics standards and improve the power factor, active PFC(Power Factor Correction) was used to rectify AC input into +400V DC output, which in turns used as input to the switching regulator.

2. INPUT

The power supply shall be capable of supplying full rated output power over free voltage ranges that are rated 100 VAC -240 VAC RMS nominal. Operating voltage : 90 VAC - 264 VAC

The power supply must be able to start up under peak loading at 90V AC. The power supply shall automatically recover from AC power loss. (Note that nominal voltages for test purposes are considered to be with +/- 1.0V of nominal).

STD_5V is a SELV standby voltage that is always present when AC mains voltage present.

3. OUTPUT

This power supply is 15 output switching power supply for PDP 42inch(Alexander). The output voltage, and current requirements for continuous operation are stated below. (table 1)

Table1. Specifications of Output Power Supplies for PDP SMPS

Output Name	Output Voltage	Output Current(Max)	Using in PDP driving
VS	+75V ~ 100V (89V)	4.5A	Sustain Voltage of Drive Board
VA	+65V ~ 80V (78V)	0.6A	Address Voltage of Drive Board
VSCAN	+65V ~ 100V (75V)	0.1A	
VSET	+80V ~ 10V (95V)	0.1A	
VE	+100V ~ 120V (110V)	0.1A	
VG	+15V	1.5 A	Driving Voltage of Fet
D12V	+12V	0.1A	
A12V	+12V	0.3A	
D6V	+6V	0.1A	IC Driving Voltage of Logic Board
A6V	+6V	0.1A	
D5V	+5V	1.0A	
D3.3V	+3.3V	4.5A	
12V AMP	+12V	1.7A	Amp Voltage of Audio Board
VT	+33V	0.003A	
STD_5V	+5V	0.6A	Stand-by for Remote Control

1) Over voltage Protection

SMPS has an over voltage detection circuit as well as a circuit which keeps a constant level of voltage. It is designed so that when an Over Voltage occurs in any part it does not affect another output part. SMPS cuts off Over Voltage in latch mode. The following tagle gives te Over Voltage protection specifications.

Table2. Over voltage Protection.

Parameter	Min	Unit
VS(85V)	100 ~	V
VA(75V)	94 ~	V
D6V	8.2 ~	V
D3.3V	4.7 ~	V

2) Short Circuit and Over current Protection.

Short-circuit of the output terminal is defined as an output impedance that is less than 300mohm. For a given SMPS, when a VS output is short-circuited, the SMPS stops operation. Even if a short-circuit occurs between the main output and the STD_5V, the SMPS does not fail. When the short-circuit is cleared, it will operate normally again. Even if a short_circuit occurs when the SMPS is operating within the range presented in Chapter 3, it will not cause a malfunction to the parts or the PCB patterns.
The following table gives Over Current protection specifications.

Table3. Over Current Protection.

Parameter	Min	Unit
VS(85V)	~	A
VA(75V)	~	A
12V	~	A
6V	~	A
D3.3V	~	A

4. Function of Board

① Remote Control

Using a 250V / 10A relay. The board makes remote control available.

② Free Voltage

The Board is designed so that the input voltage can be used within 90VAC to 264VAC.

③ Improvement of power factor

The SMPS has a power-factor compensation circuit so that the power-factor can be more than 0.9.

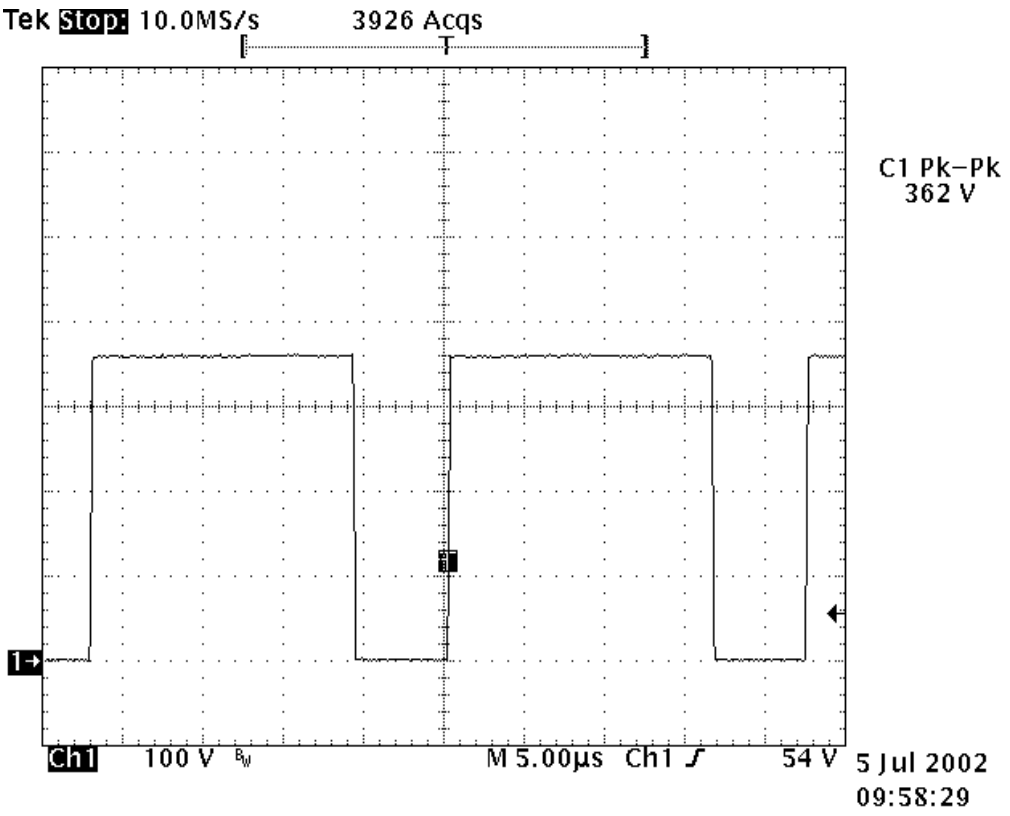
④ Protection

The SMPS has circuits which protect the product from over current, over voltage and short-circuit.

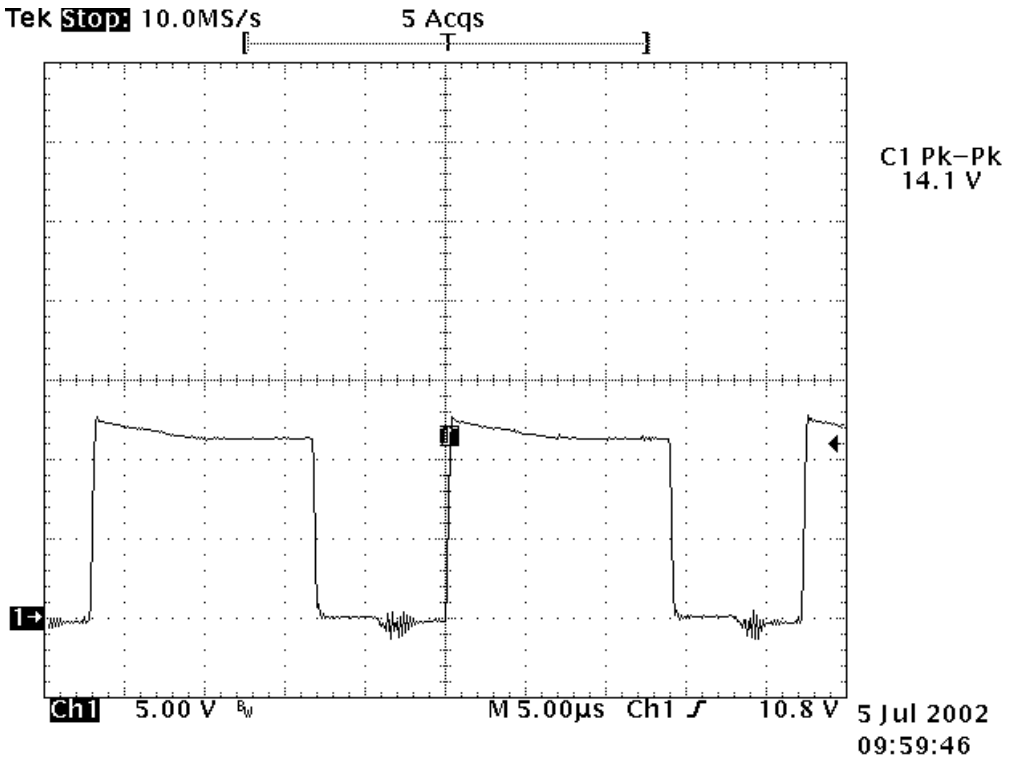
5. Part Block Diagram and Part Function.

① AC-DC Converter

The AC / DC Converter converts AC input into DC voltage using a power-factor enhancement circuit. It is designed to not only enhance the power-factor but also suppress noise. It also becomes the input for other constant voltage parts.



Picture 1. PFC Drive FET(2SK2372) Drain pulse



Picture 2. PFC Drive FET(2SK2372) Gate pulse

- Oscillator Frequency

Oscillator Frequency is determined by the values of Rt and Ct in the circuit. These values also determine the oscillation wave tilt and the off time of frequency. Osillation frequency is obtained using the following formula.

$$f_{osc} = \frac{1}{t_{RAMP}}$$

$$t_{RAMP} = C_t \times R_t \times 0.51$$

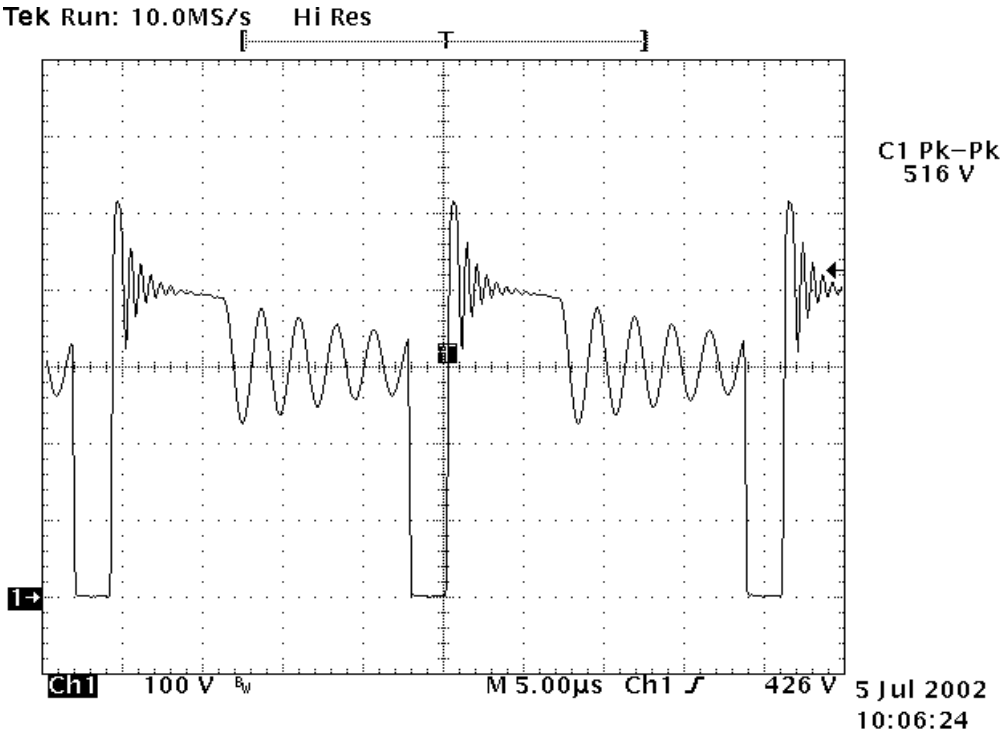
In the SMPS circuit, the oscillation frequency is as follows:

$$f_{osc} = \frac{1}{2.2nF * 20k * 0.51} = 59.417kHz$$

R_t (R59 : 1/8W 20K) , C_t (C14: MLCC 222)

② Auxiliary Power Supply

The auxiliary power supply supplies power to the remote control for activating the Micom. It operates anytime the power cord is connected to a power source and the Micom is in stand-by mode. The output in this state is called Stand-By voltage. When the ON signal is activated from the remote control, the main power supply of the SMPS starts operation.



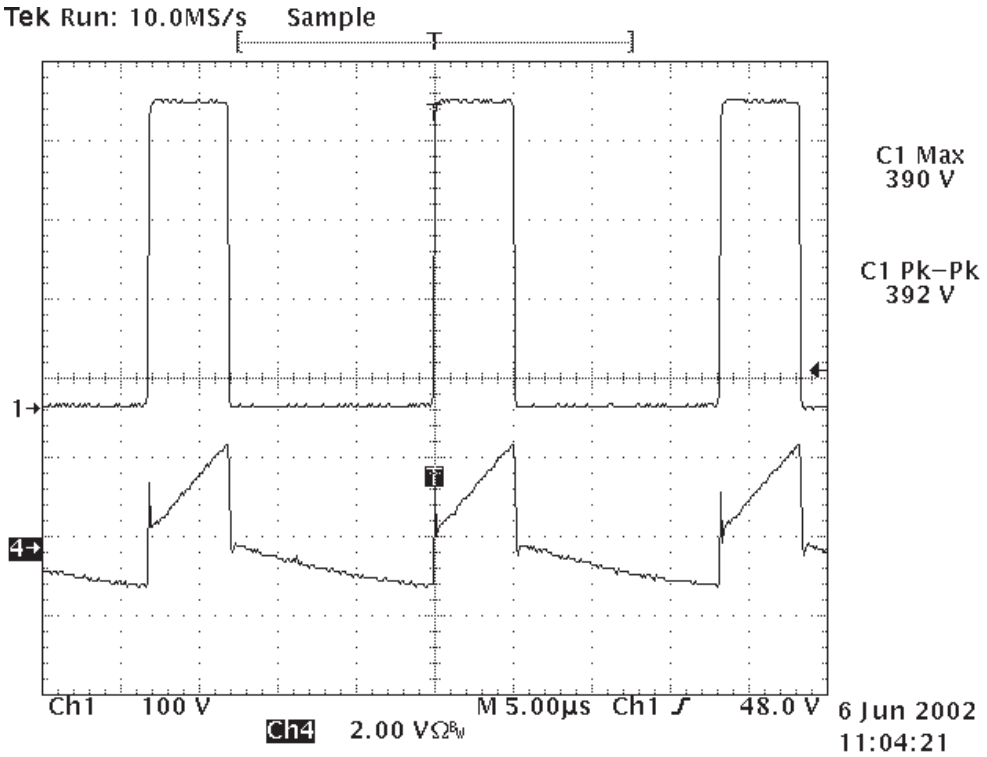
Picture 3. Standby flyback Pulse.

③ Implementation of Sustain Voltage

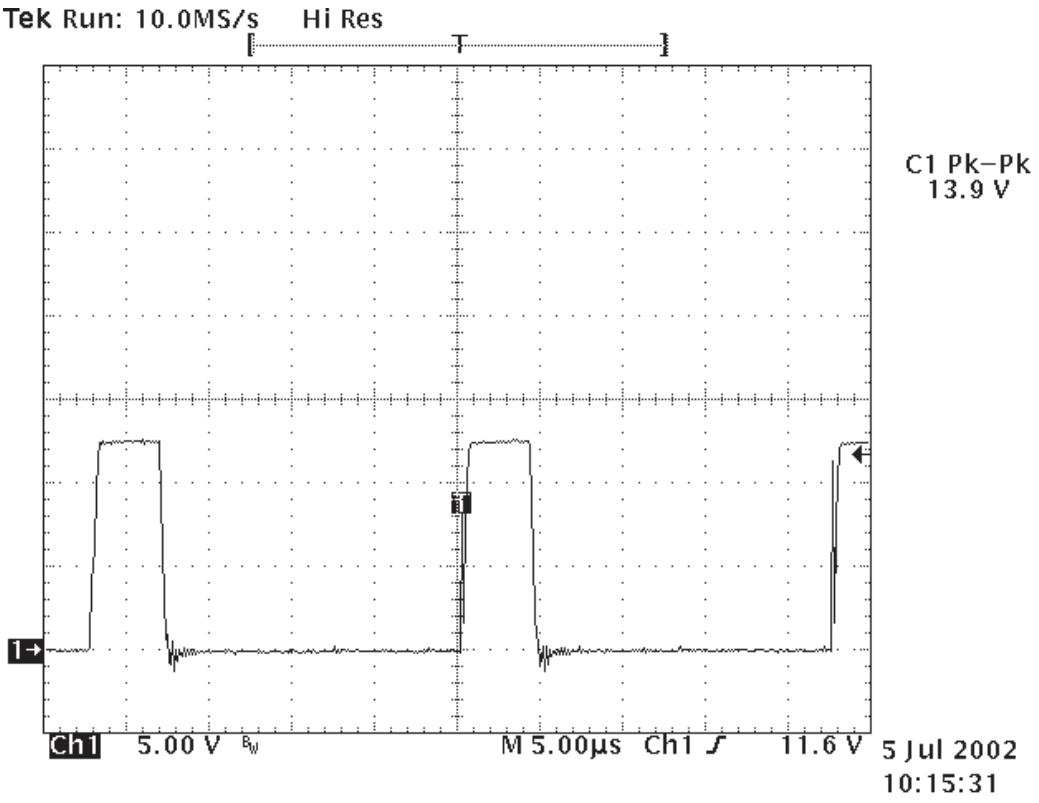
As the main part of a SMPS for PDP, sustain voltage must supply a high power, 85V/5.0A.

To comply with the specification, the Asymmetrical Half Bridge converter method was used.

At the output stage two 85V converters are connected parallel for high efficiency and reduction of system size against a single 85V converter.



Picture 4. VS Drive FET(SPW17N80C3) Drain pulse



Picture 5. VS Drive FET(SPW17N80C3) Gate pulse

- PWM SECTION (Pulse Width Modulator)

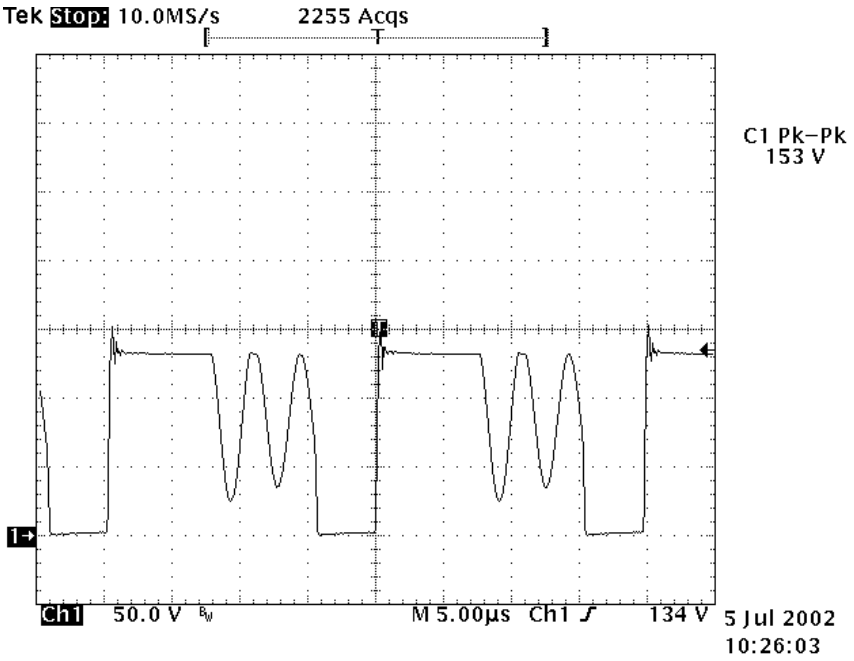
The PWM component of ML4824 is used. There are some items you should pay attention to.

The PWM component is synchronized with the PFC component mentioned above.

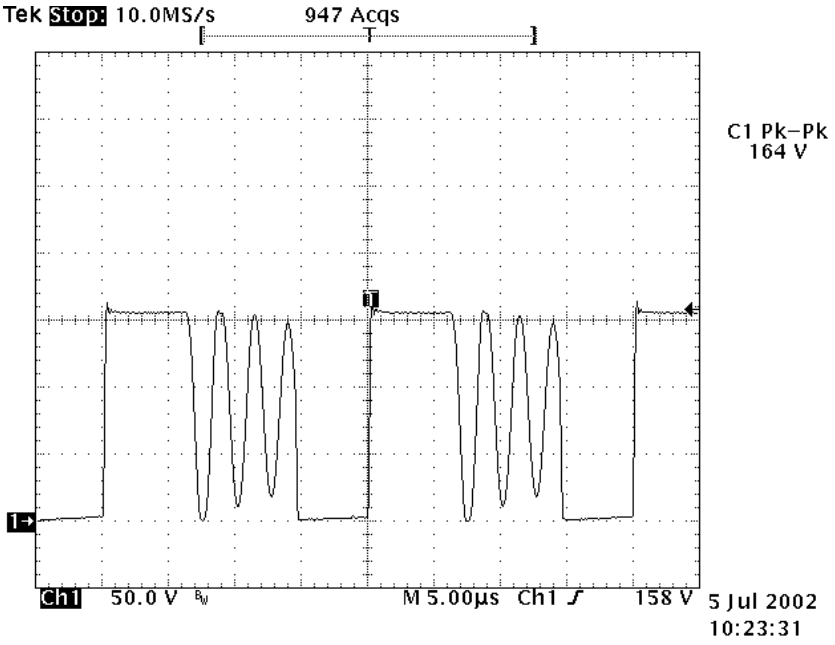
In Current Mode Operations, a PWM wave is induced via a current detection resistor or current transformer and indicates the current that flows through the output terminal.

④ DC-DC Converter

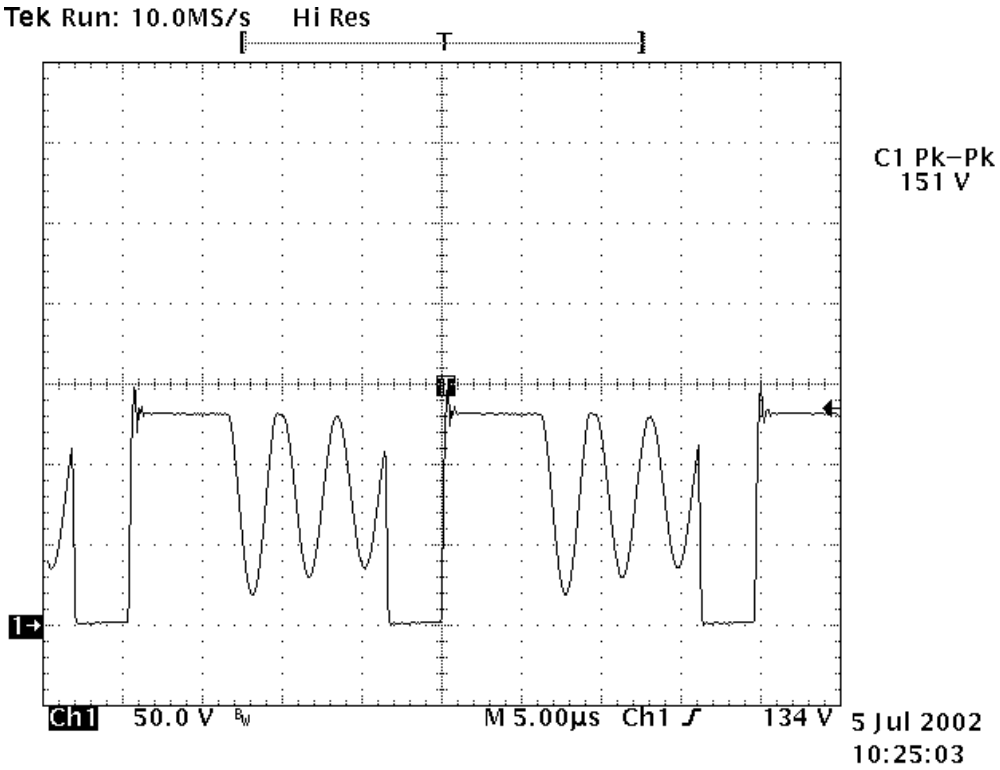
Input to VSCAN, VSET and VE are included in the VS component.



Picture 6. VSET Pulse

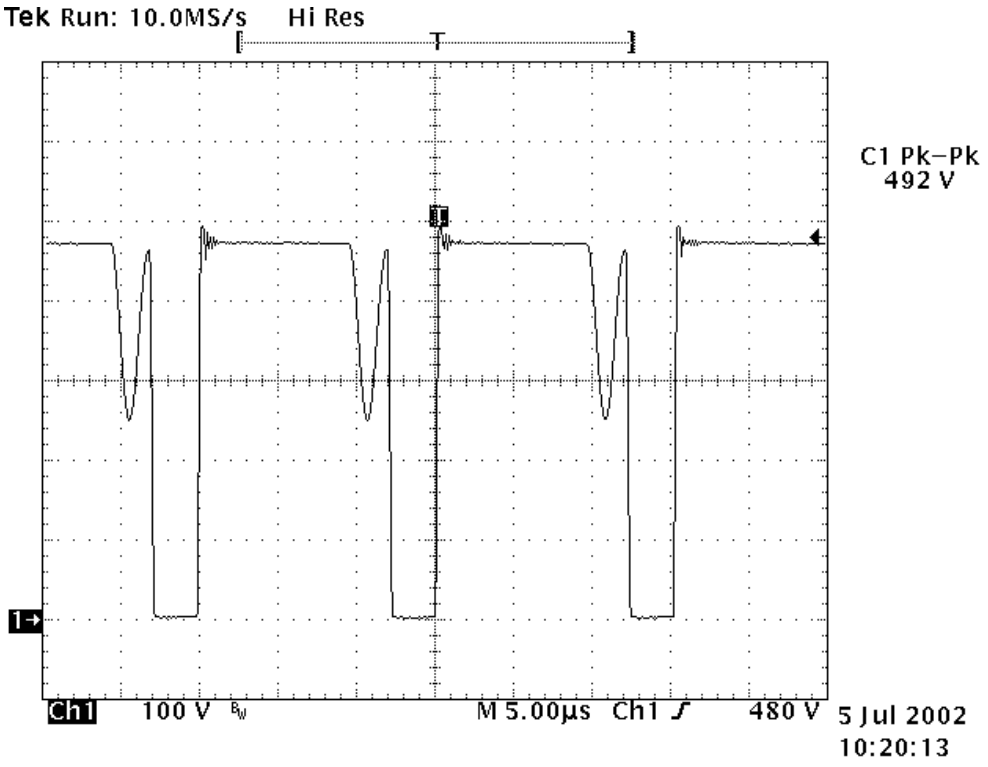


Picture 7. VE Pulse

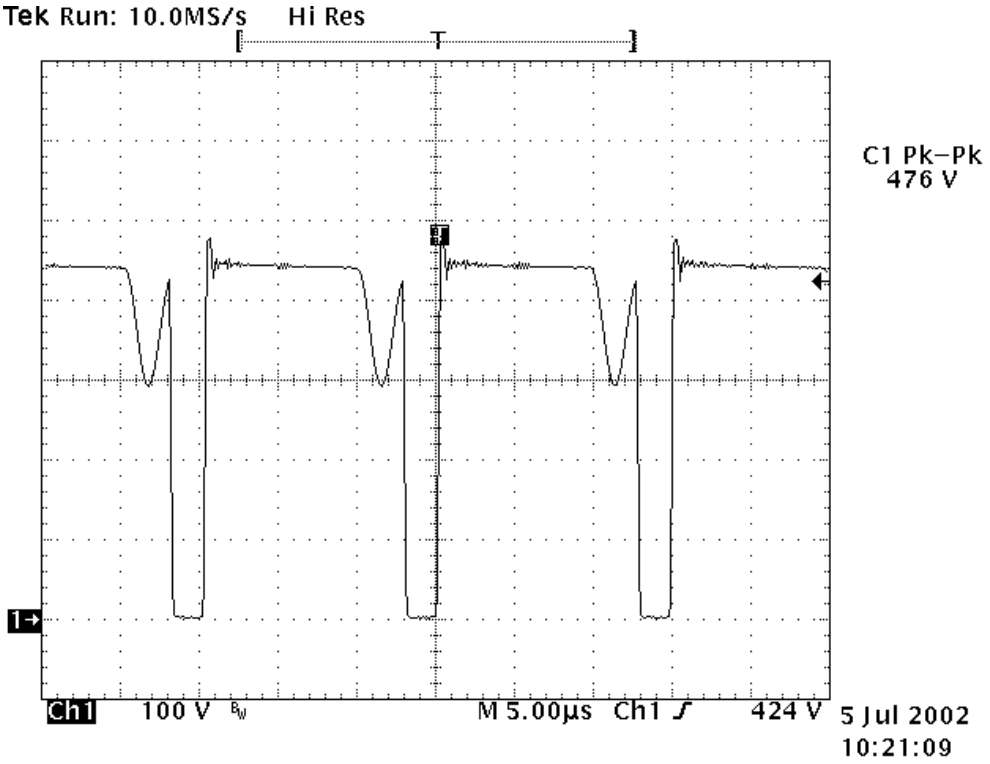


Picture 8. VSCAN Pulse

⑤ Output (VA,Multi Outputs) Pulse



Picture 9. VA Main Pulse



Picture 10. Multi Outputs Main Pulse

5-3-3 Connector Pin Assingnment

CN801(D-ANALOG)

NO	OUTPUT	SYM
1	+6V	A6V
2	RTN	
3	+12V	A12V
4	RTN	
5	+12V	12VAMP
6	+12V	12VAMP
7	RTN	RTN_AMP
8	RTN	RTN_AMP
9	+33V	VT
10	RTN	

CN802(D-DIGITAL)

NO	OUTPUT	SYM
1	+6V	D6V
2	RTN	
3	+3.3V	D3.3V
4	+3.3V	D3.3V
5	RTN	
6	RTN	
7	+12V	D12V
8		PS_ON
9	RTN	
10	+5V	STD_5V
11		THER_D

CN803(LOGIC)

NO	OUTPUT	SYM
1	+3.3V	D3.3V
2	+3.3V	D3.3V
3	RTN	
4	RTN	
5	+5V	D5V
6	RTN	
7		I^2C
8		I^2C
9		VS_ON
10	RTN	

CN804(SX)

NO	OUTPUT	SYM
1	+5.0V	D5V
2	+15V	VG
3	RTN	
4	RTN	
5	+110V	VE
6	RTN	
7	RTN	
8	+85V	VS
9	+85V	VS

CN805(SY)

NO	OUTPUT	SYM
1	+5.0V	D5V
2	+15V	VG
3	RTN	
4	+75V	VSCAN
5	RTN	
6	+60V	VSET
7	RTN	
8	RTN	
9	+85V	VS
10	+85V	VS

CN806,812(BUFFER)

NO	OUTPUT	SYM
1	+75V	VA
2	+75V	VA
3	N.C	
4	RTN	
5	RTN	

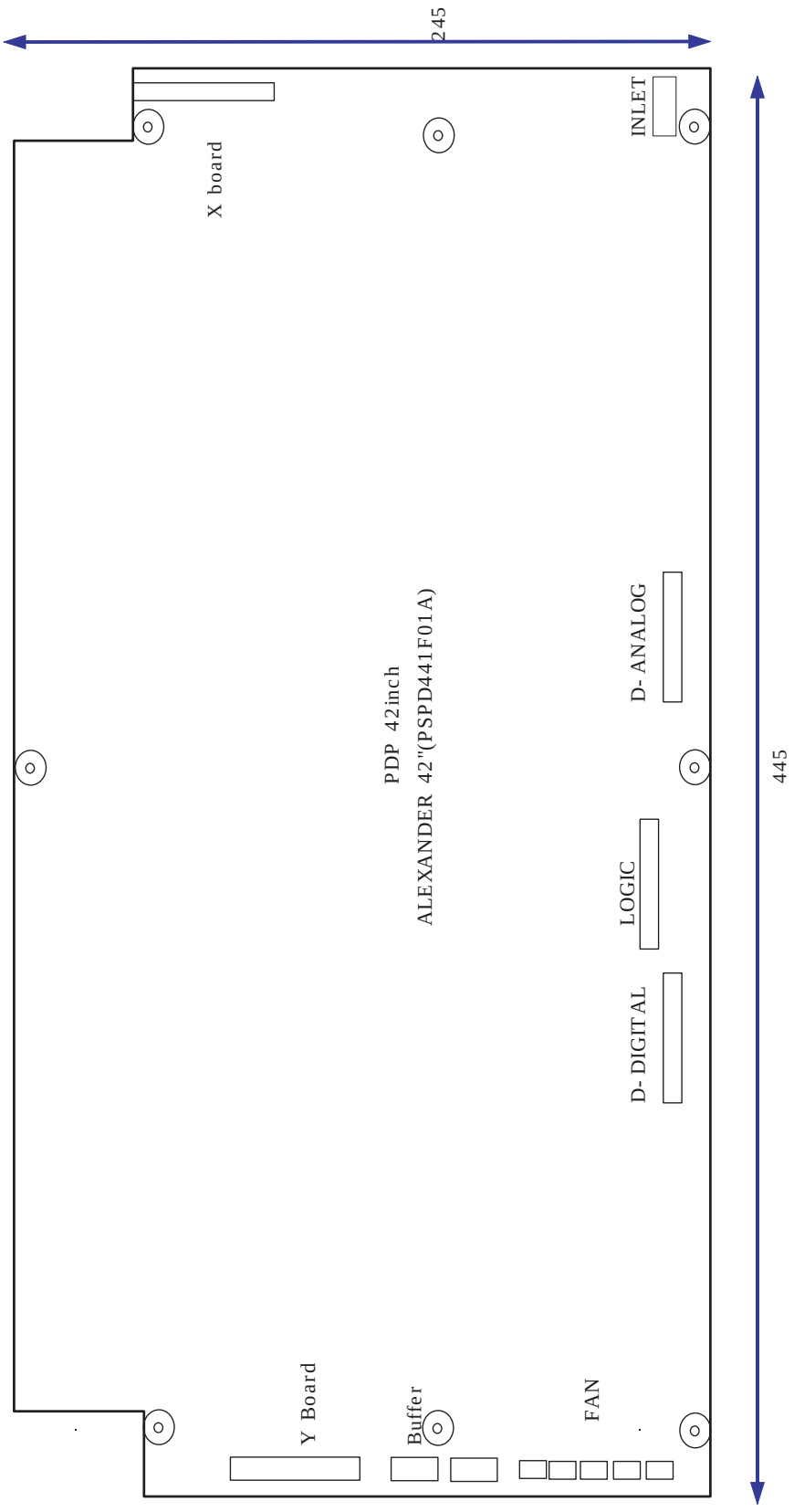
CN800(AC INPUT)

NO	INPUT	SYM
1	AC	L
2	AC	N

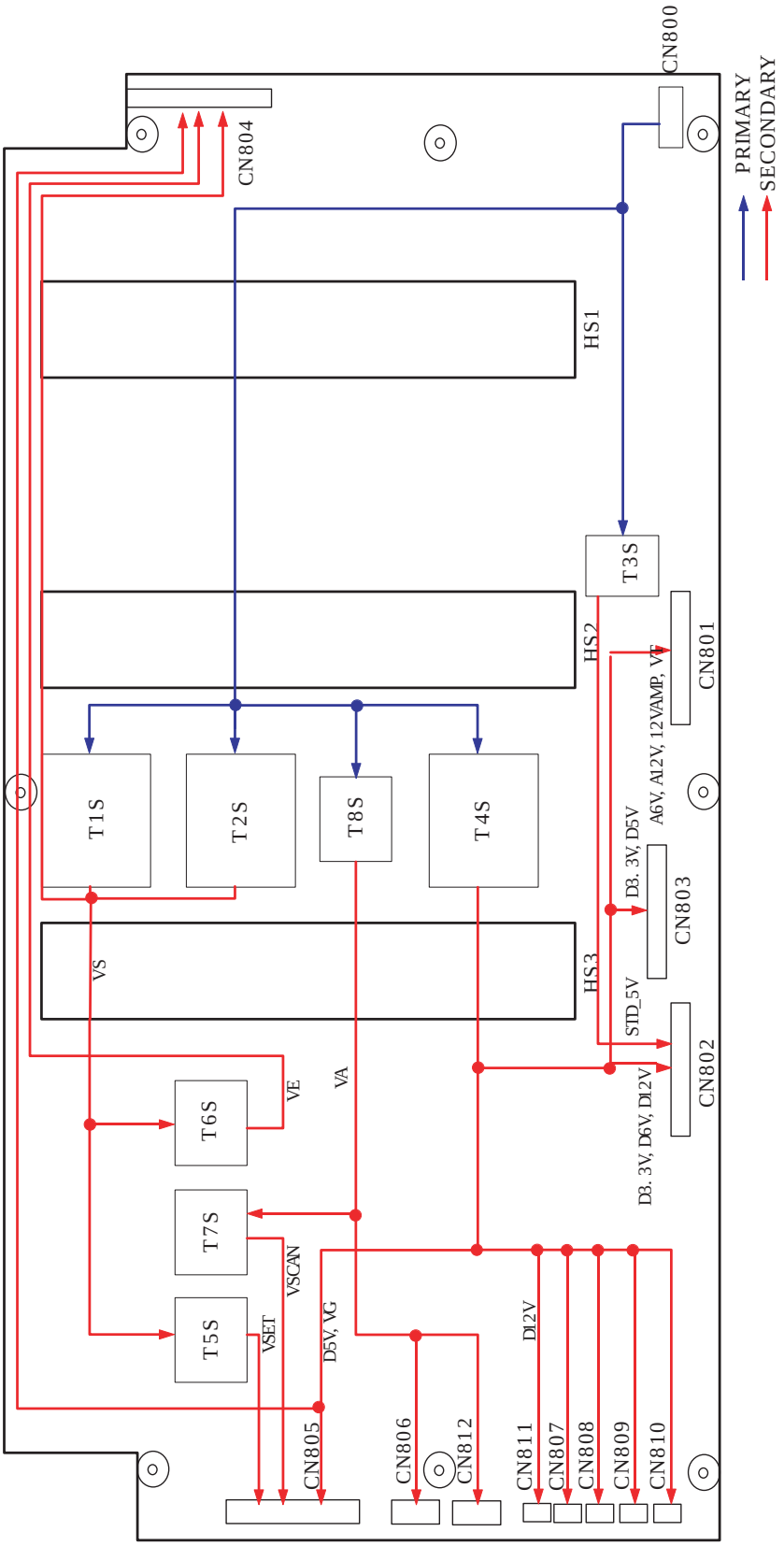
CN807,808,809,810,811 (FAN)

NO	OUTPUT	SYM
1	+12V	D12V
2	RTN	
3		FAN_D

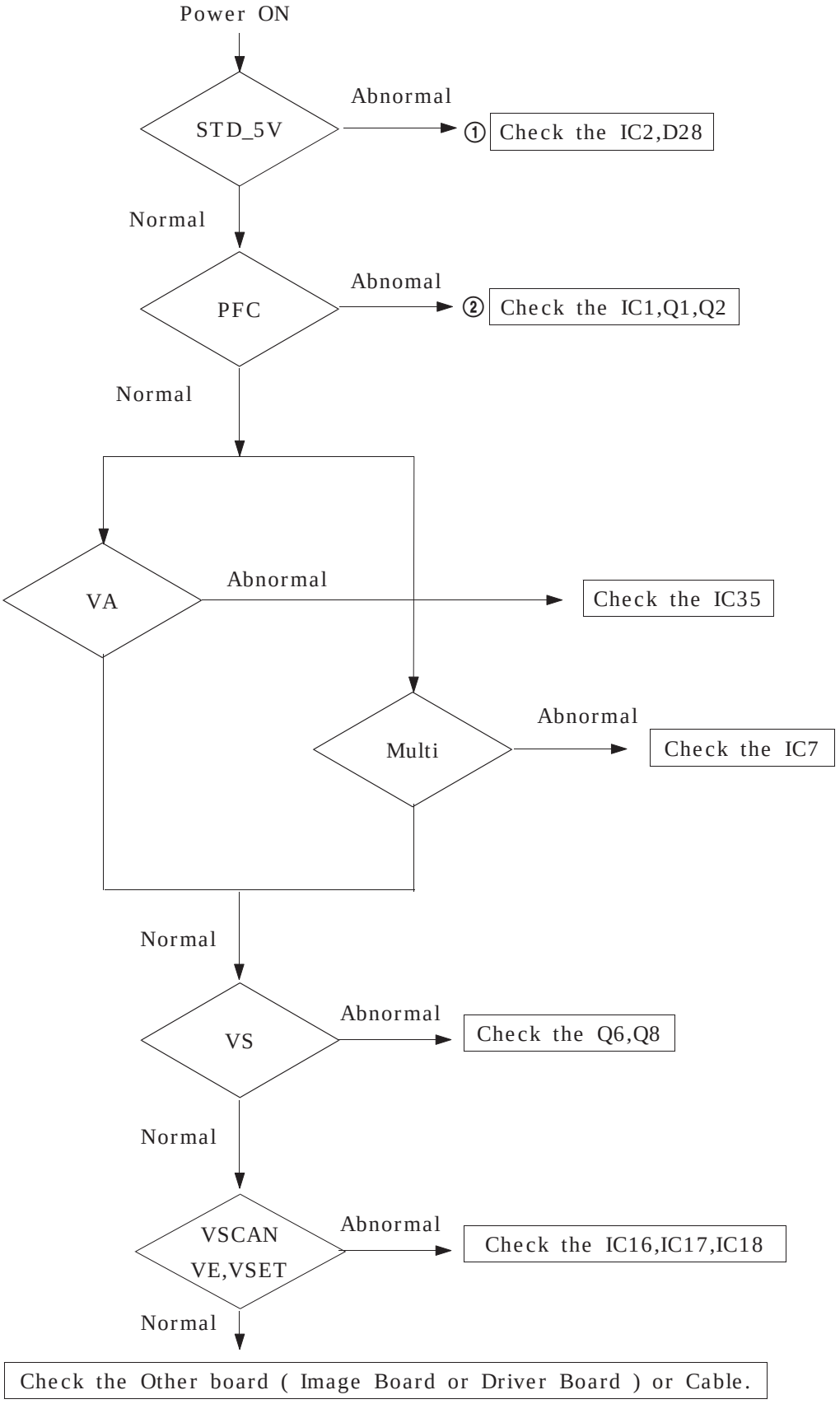
5-3-4 Power Supply Systematic Diagram and Wiring Diagram



5-3-5 Power Supply Layout



5-3-6 Trouble Shooting



5-3-7 Component Spec

Q1,Q2	SPW47N60S5	600V,47A	INFENEON	PFC Switching FET
Q6,Q8	2SK2372	500V,25A	NEC	VS FET
IC1	ML4824IP-1		FAIRCHILD	PFC,PWM Combo IC
IC2	ICE2A280	800V,2A	INFINEON	V5SB Switching IC
IC16	1L0380R	800V,3A	FAIRCHILD	VSET Switching IC
IC17				VE Switching IC
IC18				VSCAN Switching IC
IC7	KA1M0880B	800V,8A	FAIRCHILD	Multi Switching IC
IC35				VA switching IC
IC14	PQ1CG20H2Z	40V,3.5A	SHARP	D5V chopper regulator
BD1,BD3	D15XB60	600V,15A	SHINDENGEN	Bridge Diode
D10	RHRP1560	600V,15A	FAIRCHILD	PFC Diode
D41,D42	KCF16A60	600V,16A	NIHON INTER	VS Output Diode
D28	D2S4M	40V,2A	SHINDENGEN	V5SB Output Diode
D37	KCF16A60	600,16A	NIHON INTER	VA Output Diode
D209	D10LC20U	200V,10A	SHINDENGEN	12VAMP Output Diode
D203	D10LC20U	200V,10A	SHINDENGEN	A12V,D12V Output Diode
D205	MBR20100CT	100V,20A	GS	A6V,D6V Output Diode
D301	MBR20100CT	100V,20A	GS	D3.3V Output Diode
D201	BYV38	1kV,2A	TELEFUNKEN	VT Output Diode
D202	D10LC20U	200V,10A	GS	VG Output diode
RL2S	G2R-1A DC5V	DC5V	OMRON	RELAY
RL3S	G2R-1A DC24V	DC24V	OMRON	RELAY

5-4 Driver Circuit

5-4-1 Driver Circuit Overview

5-4-1(A) What is The Definition of Drive circuit?

It is a circuit generating an appropriate pulse (High voltage pulse) and then driving the panel to implement images in the external terminals (X electrode group, Y electrode group and address electrode), and this high voltage switching pulse is generated by a combination of MOSFET's.

5-4-1(B) Panel Driving Principles

In PDP, images are implemented by impressing voltage on the X electrode, Y electrode and address electrode, components of each pixel on the panel, under appropriate conditions. Currently, ADS (Address & Display Separate: Driving is made by separating address and sustaining sections) is most widely used to generate the drive pulse. Discharges conducted within PDP pixels using this method can largely be classified into 3 types, as follows:

(1) Address discharge : This functions to generate wall voltage within pixels to be lighted by addressing information to them (i.e., impressing data voltage)

(2) Sustain discharge : This means a display section where only pixels with wall voltage by the address discharge display self-sustaining discharge by the support of such wall voltage. (Optic outputs realizing images are generated.)

(3) Erase discharge : To have address discharge occur selectively in pixels, all pixels in the panel must have the same conditions (i.e., the same state of wall and space electric discharges). The ramp reset discharge section, therefore, is important to secure the drive margin, and methods most widely used to date include wall voltage controlling by ramp pulse.

5-4-1(C) Types and Detailed Explanation of Drive Discharges

(1) Sustaining discharge

Sustaining discharge means a self-sustaining discharge generated by the total of the sustaining pulse voltage (usually, 160~170V) alternately given to X and Y electrodes during the sustaining period and the wall voltage that varies depending upon pixels' previous discharge status. It is operated by the memory function (through this, the current status is defined by previous operation conditions) AC PDP basically possesses. That is, when there is existing wall voltage in pixels (in other words, when pixels remain ON), the total of wall voltage and a sustaining voltage to be impressed subsequently impresses a voltage equal to or above the discharge start voltage, thereby generating discharge again, but when there is no existing wall voltage in pixels (in other words, when pixels remain OFF), the sustaining voltage only does not reach the discharge start voltage, thus causing no discharge. The sustaining discharge is a section generating actual optic outputs used in displaying images.

(2) Address discharge

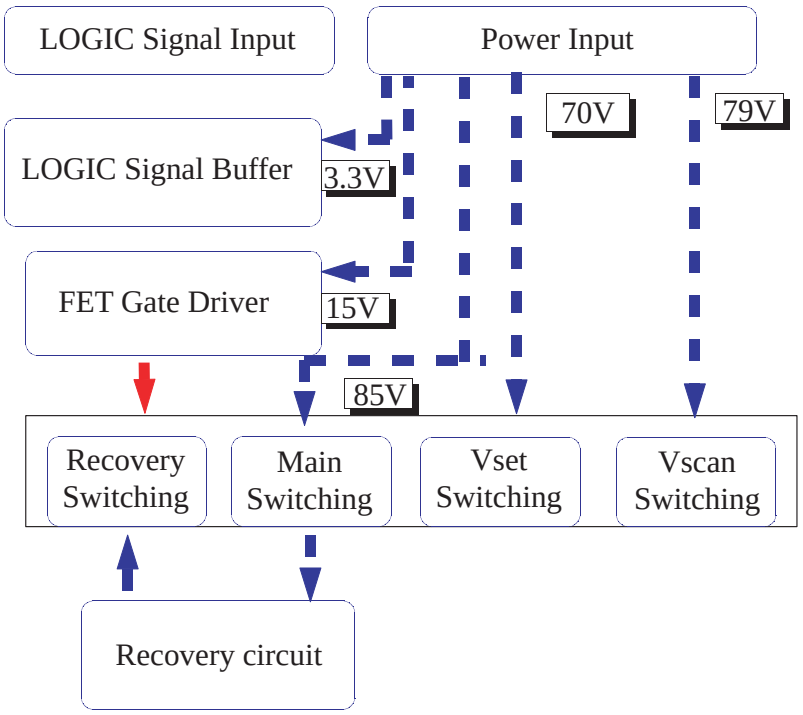
This means a discharge type generated by the difference between positive voltage of the address electrode (normally 70~75V determined by supplied Va voltage + positive wall charge) and the negative potential of Y electrode (supplied GND level voltage + negative wall charge). The address discharge serves to generate wall voltage in pixels where images are to be displayed (that is, discharge is to be generated) prior to the sustaining discharge section. Namely, pixels with wall voltage by the address discharge will generate sustaining discharge by the following sustaining pulses.

(3) Erase discharge

The purpose of resetting or erase discharge is to make even wall voltage in all pixels on the panel. Wall voltage, which may vary depending upon the previous sustaining discharge status, must be made even. That is, wall voltage generated by the sustaining discharge must surely be removed, by making discharges and then supplying ions or electrons. Wall voltage can be removed by making discharges and then setting a limitation on time for opposite polarity charging of the wall voltage or generating weak discharge (Low voltage erasing) to supply an appropriate quantity of ions or electrons and keep polarities from being charged oppositely. The weak discharge (Low voltage erasing) methods, which have been known to date, can largely be into two types: 1) the log pulse adopted by most companies including F Company, and 2) the ramp pulse adopted by Matsushita. In both two methods, impression is made with a slow rising slope of the erasing pulse. Because the total of the existing wall voltage and a voltage on the rising pulse must be at least the drive start voltage to generate discharges, external impressed voltage is adjusted based on the difference in wall voltage between pixels. And, weak discharge is generated because of a small impressed voltage.

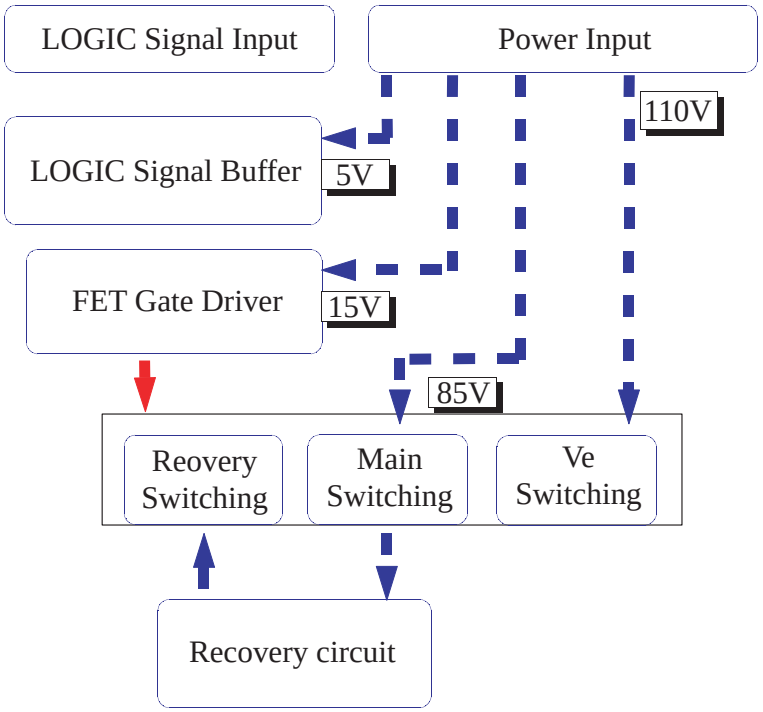
5-4-1(D) Drive Board Block Diagram

① Y



Picture. Drive Y-Board

② X



Picture. Drive X-Board

③ Required elements for operating the drive board

1. Power

- Supplied from the power board. Optimized value may differ slightly from the following value.

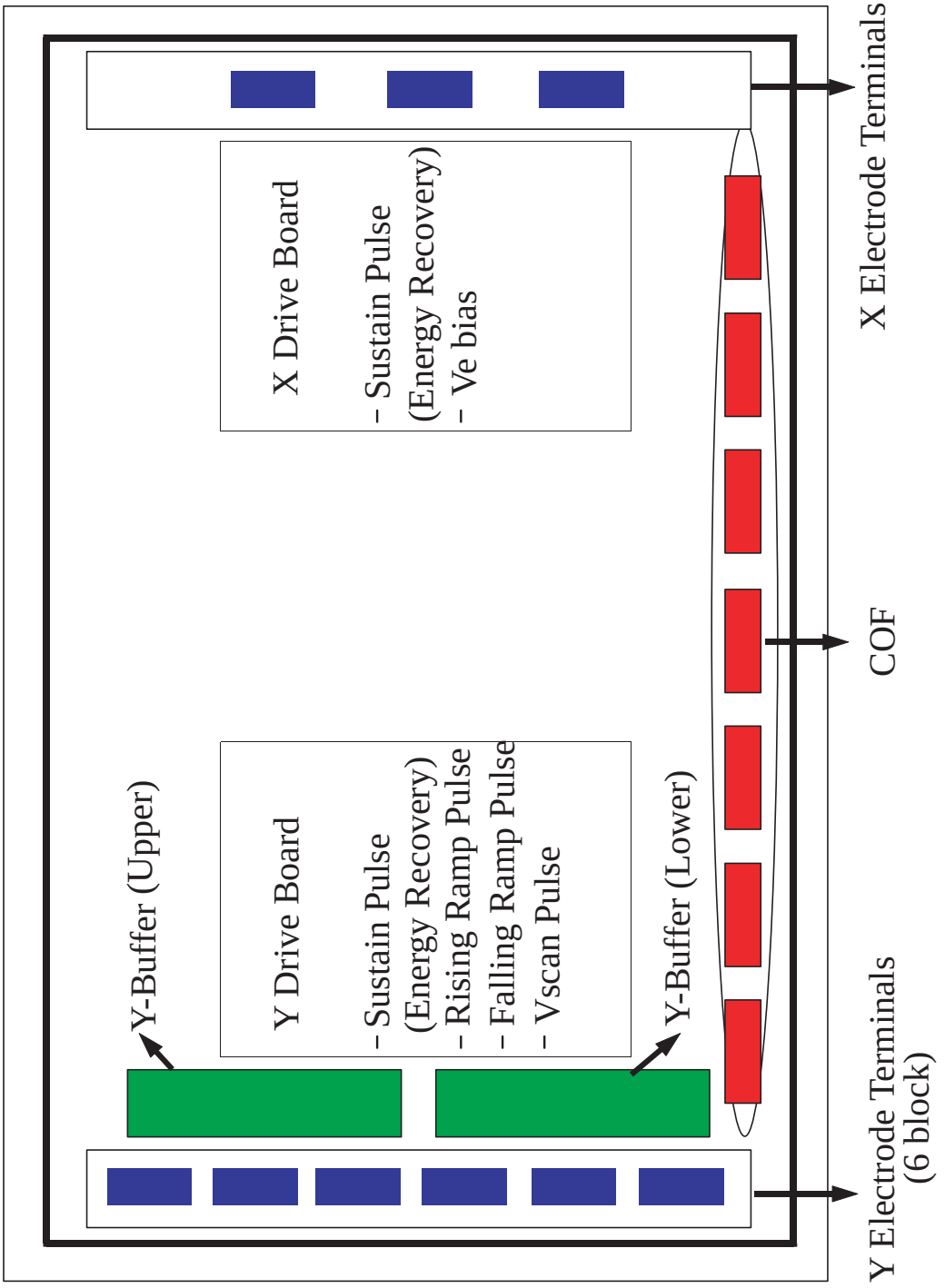
a) Vs	: 85V	- Sustain
b) Vset	: 60V ~70V	- Y Rising Ramp
c) Ve	: 110V	- Ve bias
d) Vscan	: 70V ~80V	- Scan bias
e) Vdd	: 3.3V	- Logic signal buffer IC
f) Vcc	: 15V	- FET Gate drive IC

2. Logic Signal

- Supplied from the logic board
- Gate signal of each FET

5-4-1(E) Drive Circuit's Operational Block Diagra m

- Functions of Boards



① X Board

Connected to the X terminals on the panel. Maintains
1) the sustain voltage waveforms(including ERC) and
2) the Ve bias during scan time

② Y Board

Connected to the Y terminals on the panel. Maintains
1) the sustain voltage waveform(including ERC)
2) the Vscan bias, and generates
3) the Y rising/falling ramp waveform.

③ Y Buffer Board(Upper, Lower)

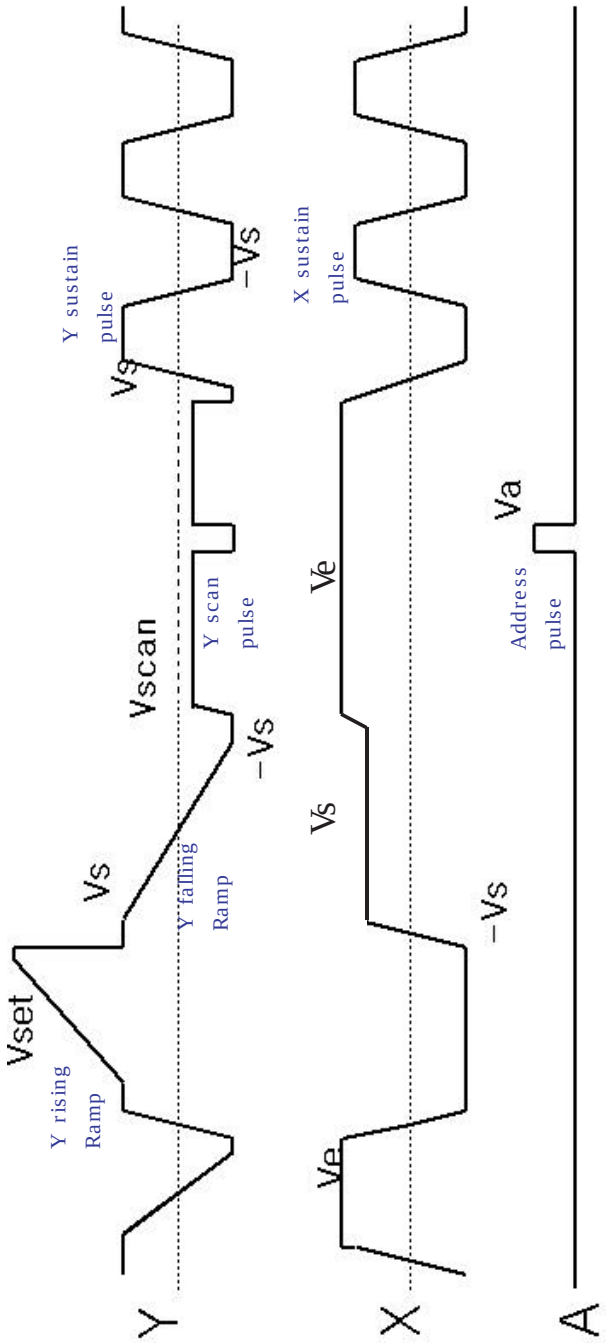
Applies the scan waveform to the Y terminals. Consists of two boards, the upper and lower board. In preparation for the SD level, four scan driver ICs (STMicroelectronics's STV7617:64 or STV7610A:963 outputs). When a single scan occurs, 7COFs are required.

④ COF

Utilizes the Va pulses on the address electrodes to form an address discharge by using the differences between the beamed pulses occurring on the Y electrodes. It is manufactured in the COF form. Each COF consists of data drive ICs (STMicroelectronics's STV7610A: 96 outputs). When a single scan occurs, 7 COFs are required.

5-4-2 SPECIFICATION OF DRIVE PULSES

5-4-2(A) DRIVE PULSES



A1, 2.	Address(=Data) Electrode
X	Common & Sustain Electrode
Y1, 2. . . .	Scan & Sustain Electrode

Vs	85V	Ve	110V
Vset	70V	Va	79V
Vscan	79V		

5-4-2(B) FUNCTIONS OF PULSES

① Y rising ramp pulse

When an external voltage of about 390V~400V is applied on the Y electrode during the Y Rising Ramp time and each gap voltage reaches the discharge sparkover voltage, a weak discharge begins. While the weak discharge is maintained, negative wall charges are accumulated on the Y electrode and positive wall charges are accumulated on the X and address electrodes, respectively.

② Y Fallimg ramp pulse

During Y rising ramp period, weak-discharge begins when external voltage of about 390V~400V is impressed to Y electrode, and each gap voltage is equal to discharge start voltage. Sustaining the weak-discharge, positive wall charge is accumulated in X electrode and address electrode, and negative wall charge is accumulated in Y electrode of the entire panel.

③ Y Scan Pulse

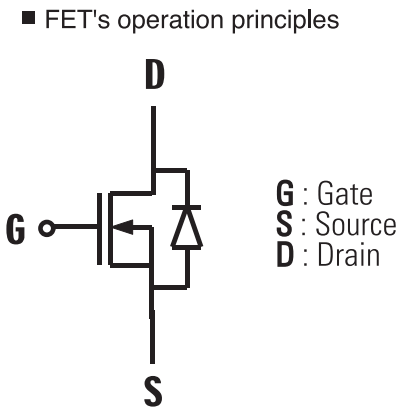
Also referred to as Beam Pulse. Selects the Y electrodes line by line. During this process, the Vscan is called Scan Bias Voltage. About 70V are applied to the electrode line to which Vscan voltage was applied, and the 0V (GND) voltage is applied to the other electrodes. However, since all negative charges are accumulated on the Y electrodes due to the application of ramp pulses and positive wall charges are accumulated on the address electrodes, the cells to which address pulses (70V~75V) are applied have more voltage than the discharge sparkover voltage and thus generate address discharges. Since the beam pulse and the data pulse should be applied one line at a time, the PDP address time is therefore very long.

④ 1st Sustain Pulse

The Sustain Pulse always starts from the Y electrode, because positive wall charges are formed on the Y electrodes when an address discharge occurs. Since the wall charge formed by an address discharge is usually less than the wall charge formed by a sustain discharge, the first discharges have a low strength and are stabilized after 5~6 discharges, though it may differ depending on the structure of the electrodes and the environmental conditions. Hence, the reason to maintain the first sustain-pulses for a long time is to form a stabilized first discharge and generate as many wall charges as it possibly can.

5-4-2(C) PRINCIPLES OF FET'S OPERATION AND HIGH VOLTAGE SWITCHING

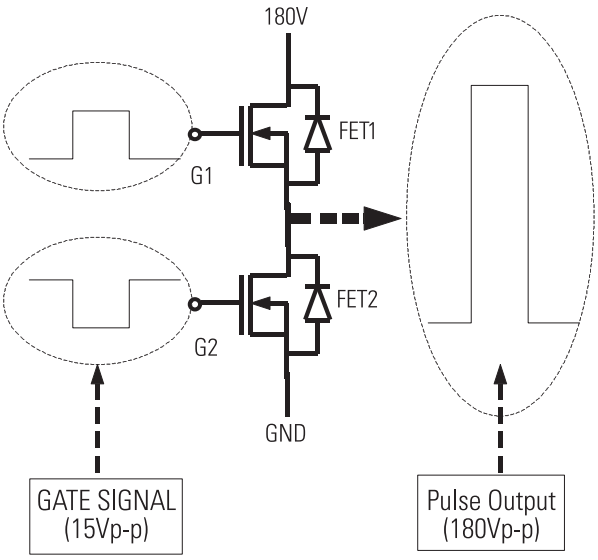
u FET's operation principles



(1) With signal impressed on the gate (Positive voltage), FET gets short-circuited (a conducting wire of zero (0) resistance); and

(2) With no signal impressed on the gate (GND), FET gets open-circuited (a non-conducting wire of ∞ resistance).

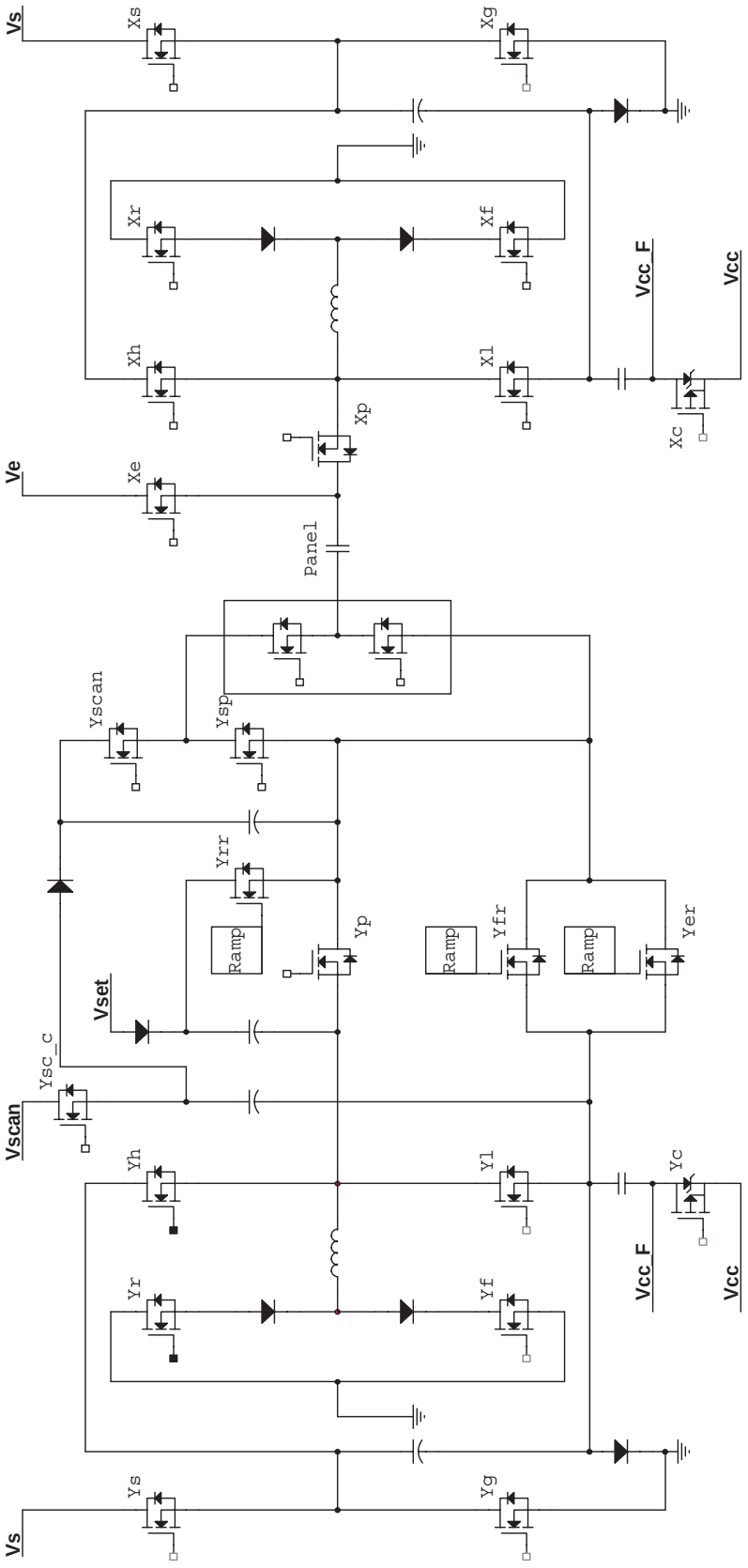
u FET's high voltage switching principles



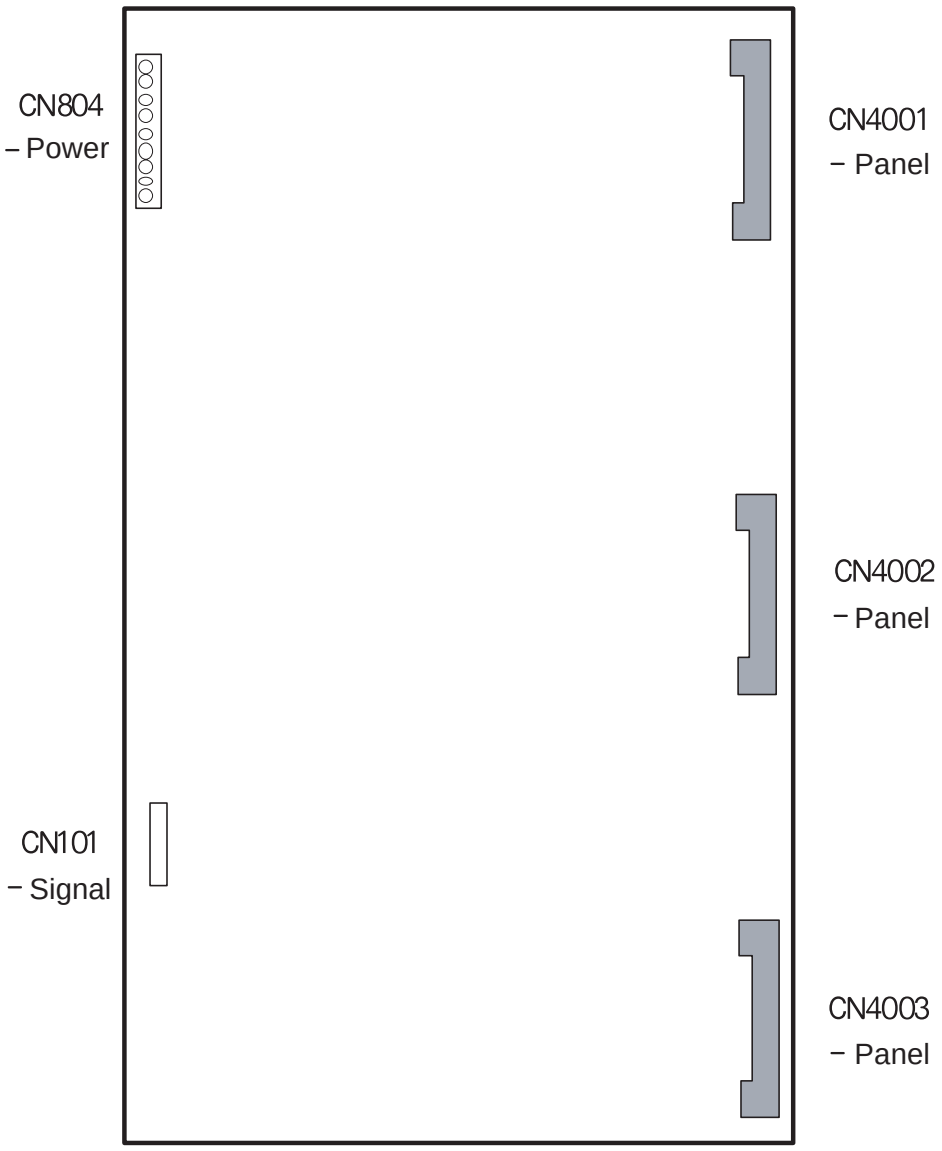
(1) With no signal impressed on G1, FET1 gets open-circuited, and with signal impressed on G2, FET2 gets short-circuited, thereby causing GND to be outputted to output terminals.

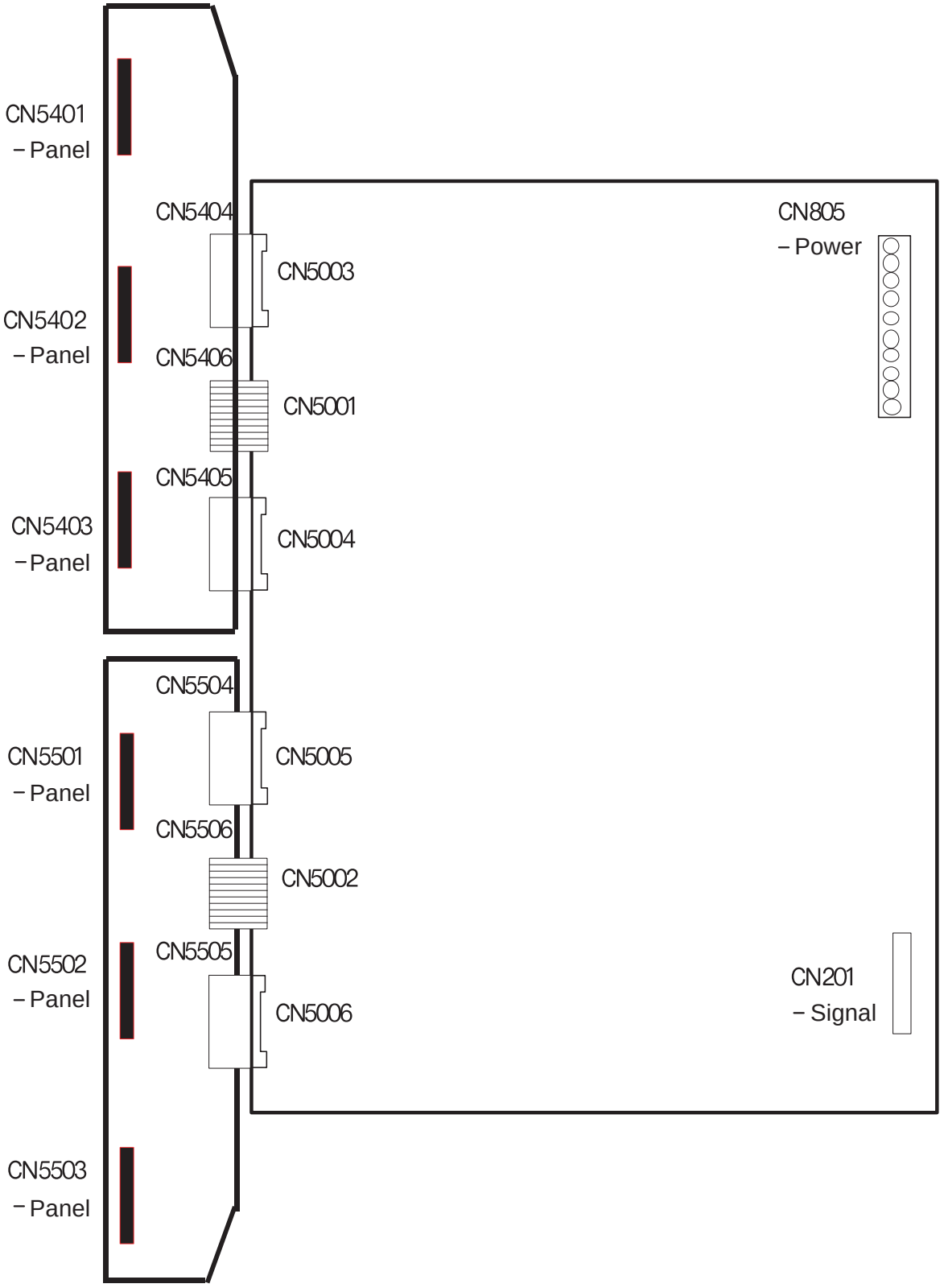
(2) With signal impressed on G1, FET1 gets short-circuited, and with no signal impressed on G2, FET2 gets open-circuited, thereby causing 180V to be outputted to output terminals.

5-4-2 (D) DRIVER CIRCUIT DIAGRAM



5-4-2(E) DRIVER BOARD CONNECTOR LAYOUT

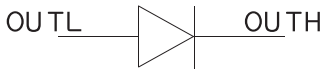



CN5401
– Panel
CN5404
CN5003
CN805
– Power
CN5402
– Panel
CN5406
CN5001
CN5405
CN5403
– Panel
CN5004
CN5504
CN5501
– Panel
CN5005
CN5506
CN5002
CN5505
CN5502
– Panel
CN5006
CN201
– Signal
CN5503
– Panel

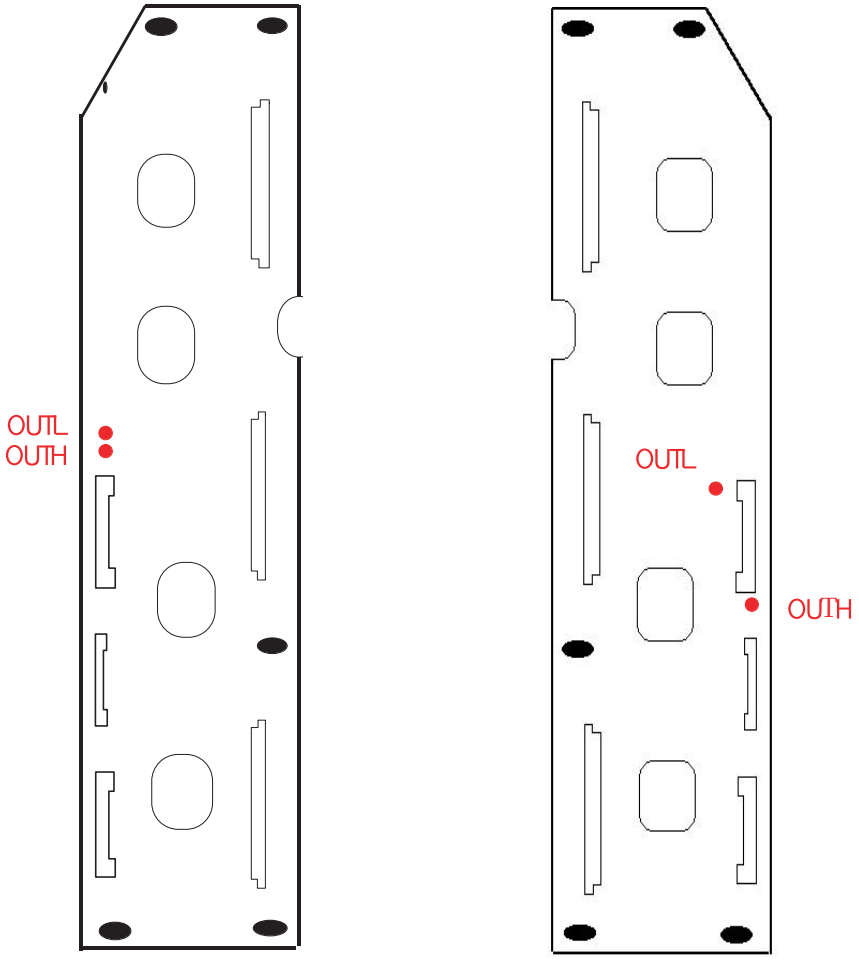
5-4-2(F) DRIVER BOARD TROUBLESHOOTING

① Y Buffer

- To check whether the Y buffer is operating normally, first check the operational status of the Y Main.
- Disconnect the connectors from the Y Main and Y buffer.
- Then check the line between OUTL and OUTH using a diode (diode ccheck) and ensure that the forward voltage falling is between 0.4V~0.5V.

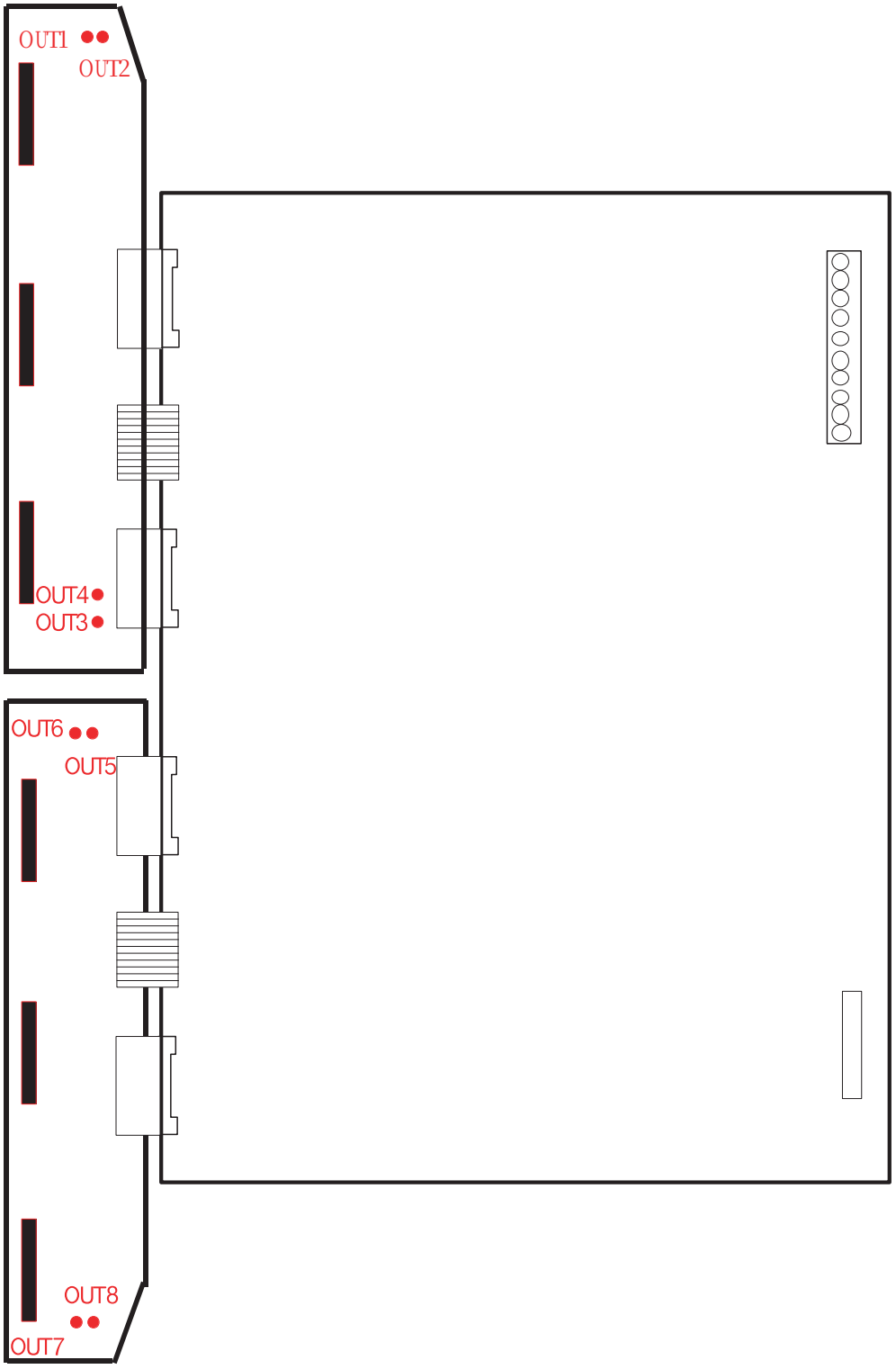


- Also, the resistance between the two terminals should be more than several k ohms.



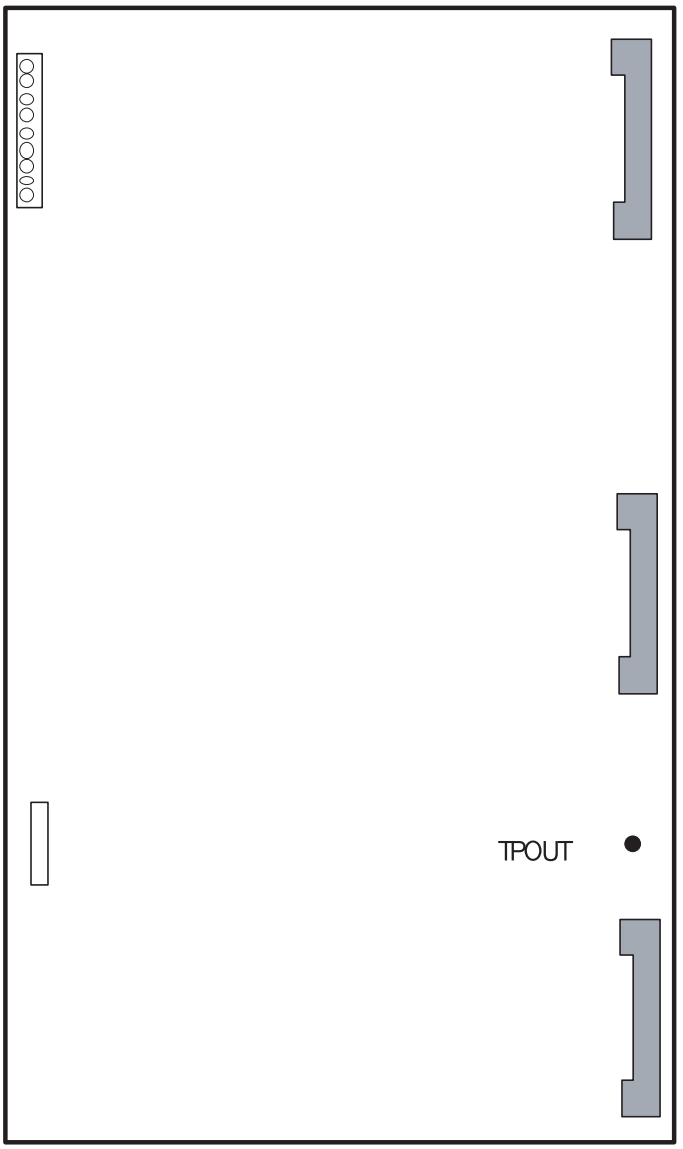
② Y Main

- Connect the Y Main to the Y buffer and apply power. Ensure that at least one of the OUT1~8 values of the Y buffer is the same as one of the values shown on Attachment 1.



③ X

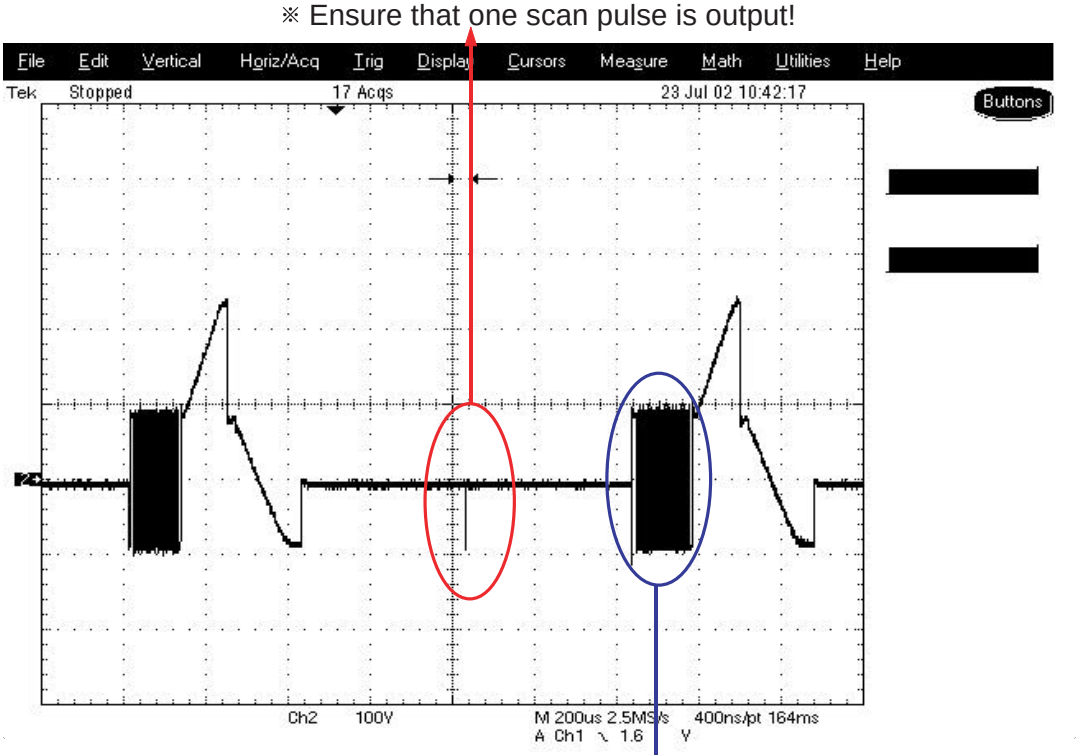
- Ensure that the TPOUT outputs on the X board match those in Attachment 2 when the power is applied.



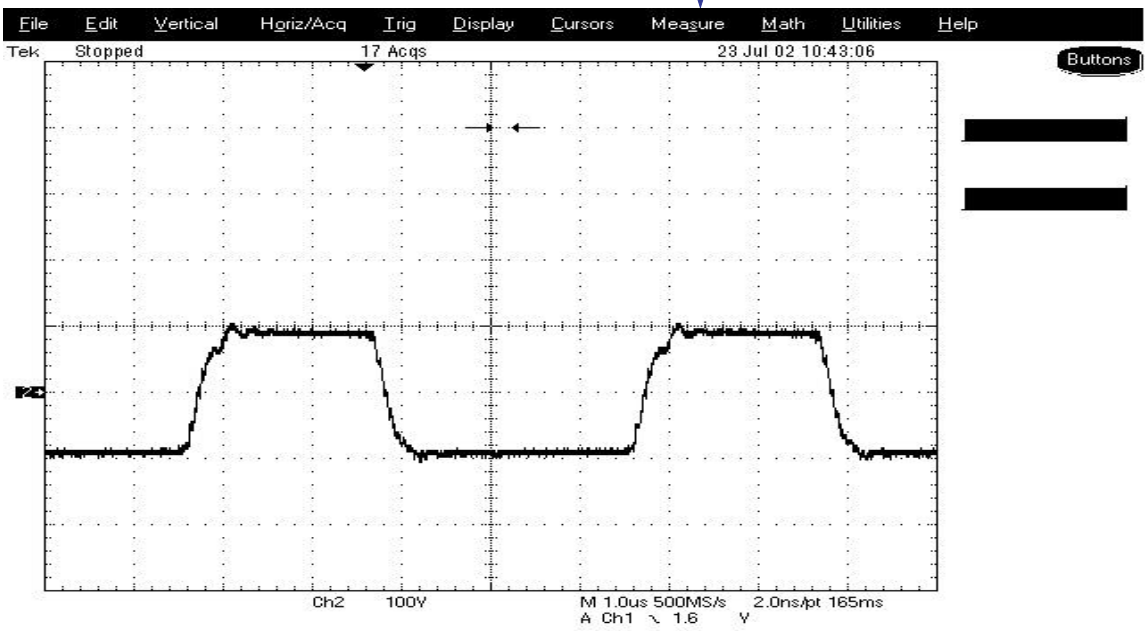
Attachment # 1

■ Y Output Waveform

※ Ensure that one scan pulse is output!



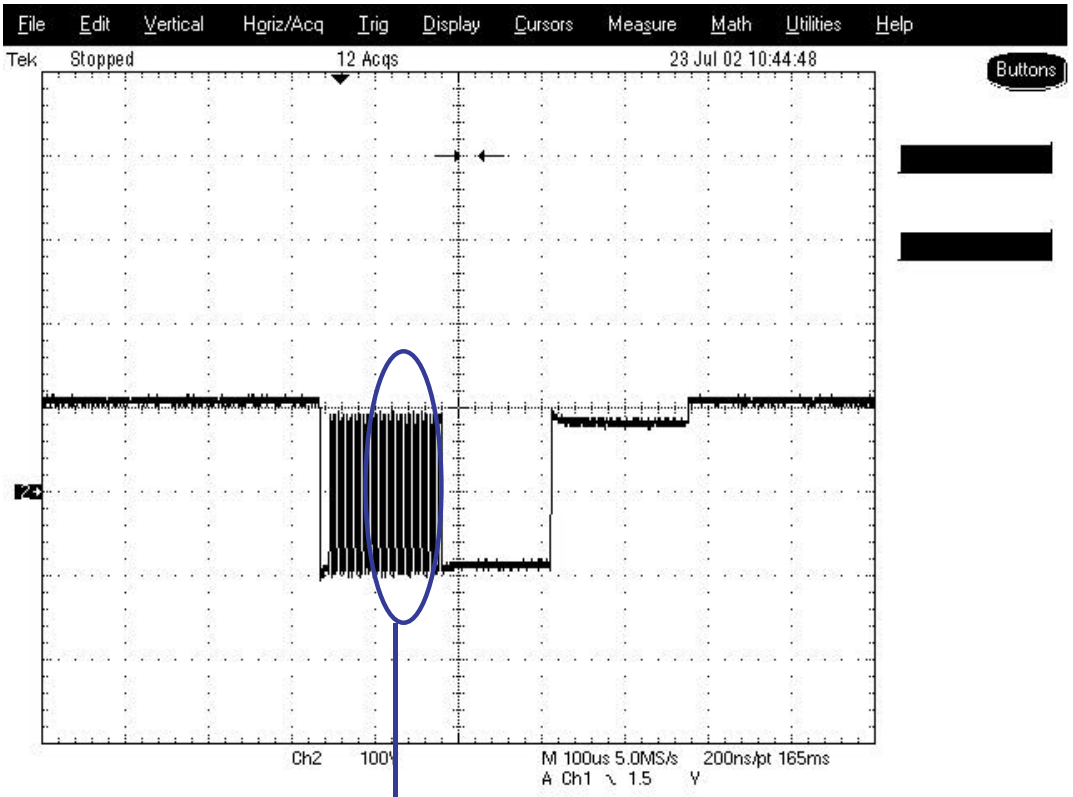
Y Output Waveform (200us/div, 100V/div)



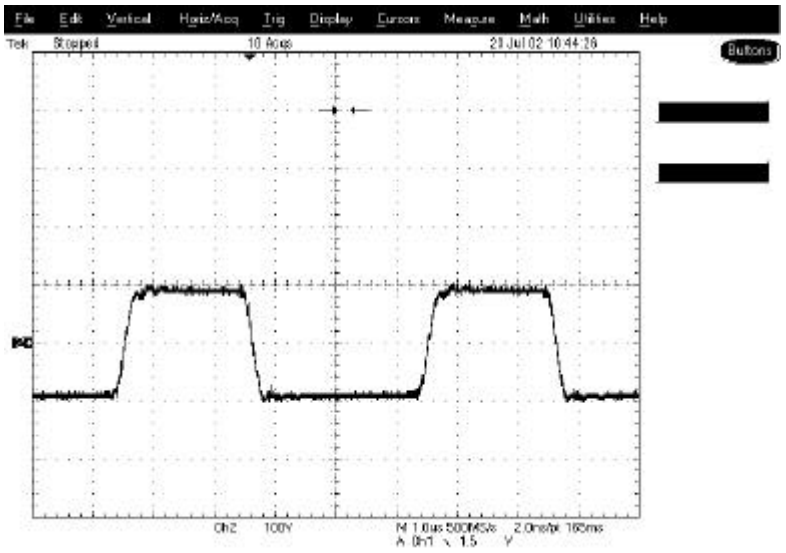
1us/div, 100V/div

Attachment # 2

■ X Output Waveform



X Output Waveform (100us/div, 100V/div)

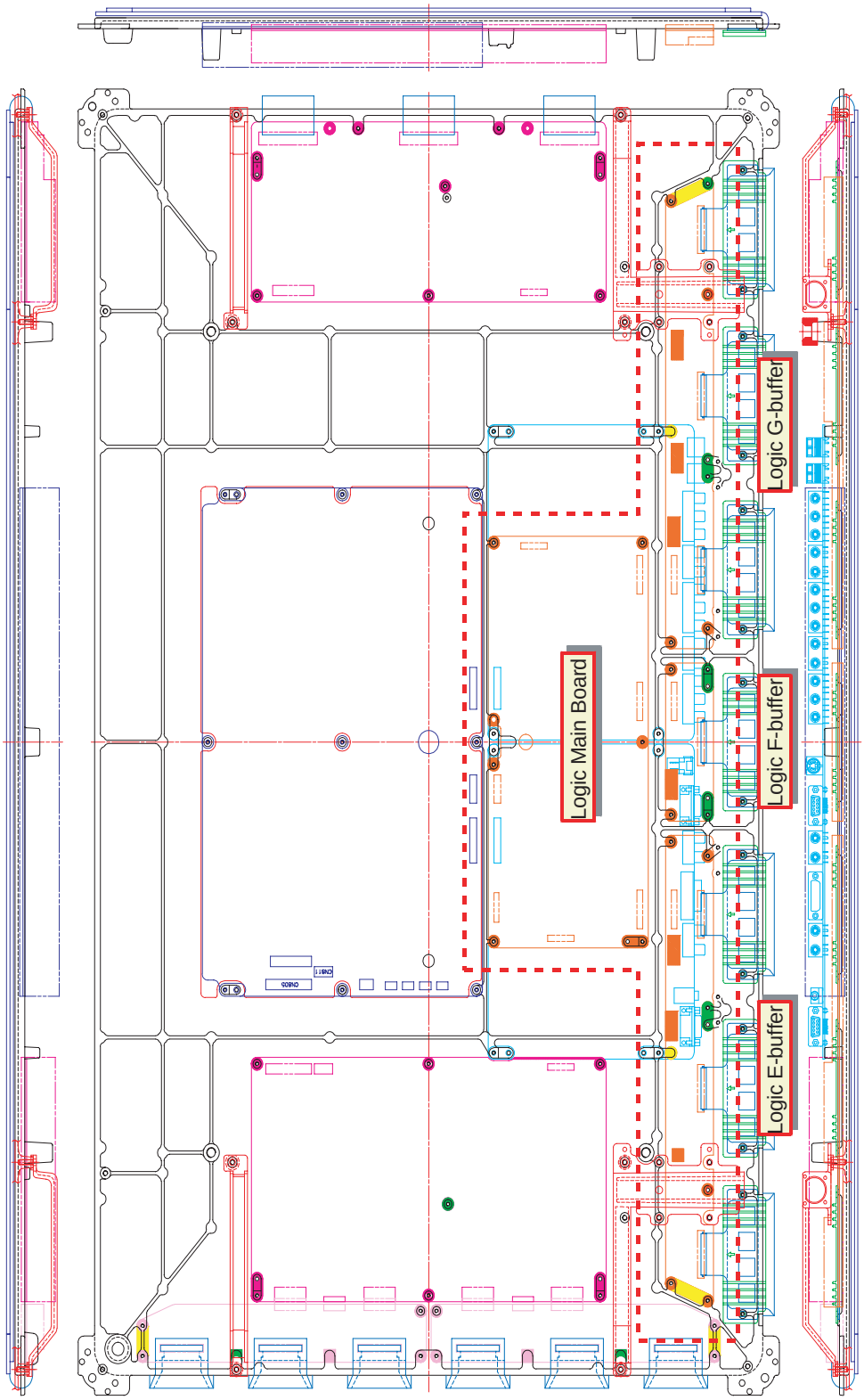


1us/div, 100V/div

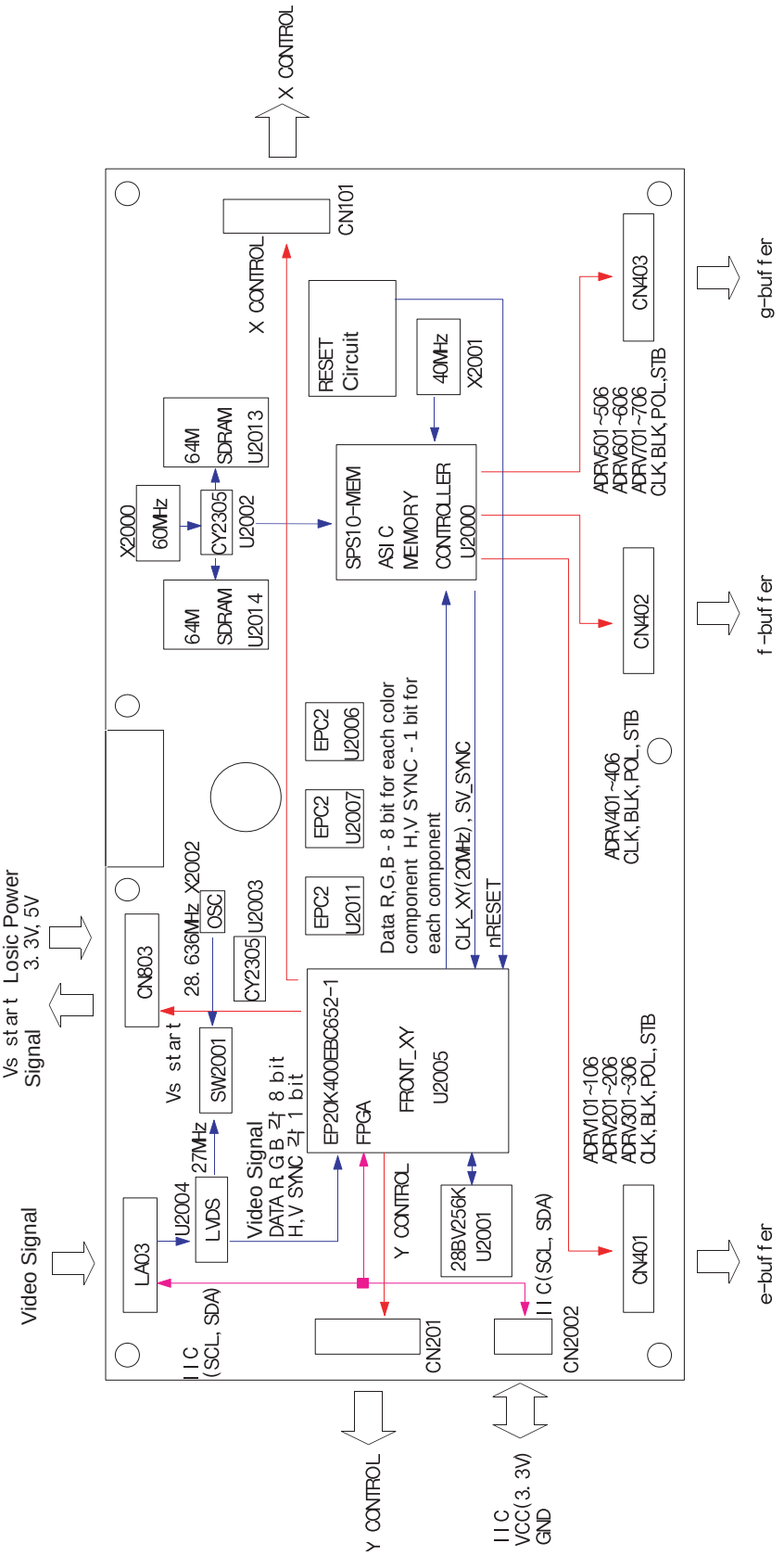
5-5 Logic part

5-5-1 Description of the Logic Board

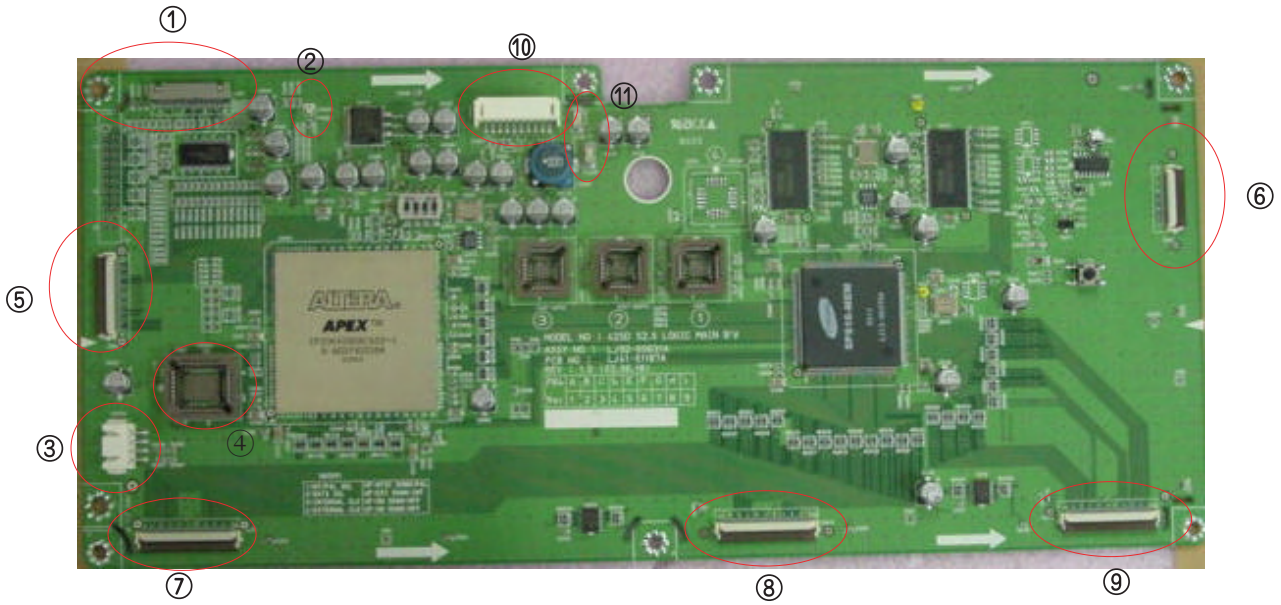
5-5-1(A) 42" SD S2.0 Board Layout



5-5-1 (B) Chart of Logic Board Signal Flow



5-5-1 (C) Name of the Major Parts of the Logic Board and Terminology



NO	Name	Function
1	LVDS Connector	Receives LVDS-encoded RGB,H,V,DATAEN, and DCLK input from video board.
2	Operation LED	Shows whether the Sync and Clock signals are entering the logic board normally. (Normal status: blinks once every second)
3	I²C Connector	Connects the key scan board which checks and adjusts the 256K data.
4	256k	EEPROM which saves the gamma table, APC table, drive waveform timings and other options.
5	Y Connector	Outputs the Y drive board control signals.
6	X Connector	Outputs the X drive board control signals.
7	CN401(E-Address Buffer Connector)	Outputs the address data and control signals to the E-buffer board.
8	CN402(F-Address Buffer Connector)	Outputs the address data and control signals to the F-buffer board.
9	CN403(G-Address Buffer Connector)	Outputs the address data and control signals to the G-buffer board.
10	Power Connector	Receives the power input (5V) for the logic board.
11	Power Fuse	Fuse attached to the power input part (5V) of the logic board.

5-5-1 (D) description of Logic Board

The Logic Board consists of the logic main board, which processes video signals and generates and outputs the address driver output signals and the XY drive signals, and the buffer board, which buffers the address driver output signals and transmit them to the address driver IC (COF Module).

Logic Board		Function	Remarks
Logic Main		- Processes video signals (WL, error diffusion, APC). - Outputs address driver control signals and data signals to the buffer board. - Outputs XY drive board control signals.	
Buffer Board	E Buffer board	Transmits data and control signals to the bottom left COF.	
	F Buffer board	Transmits data and control signals to the bottom center COF.	
	G Buffer board	Transmits data and control signals to the bottom right COF.	

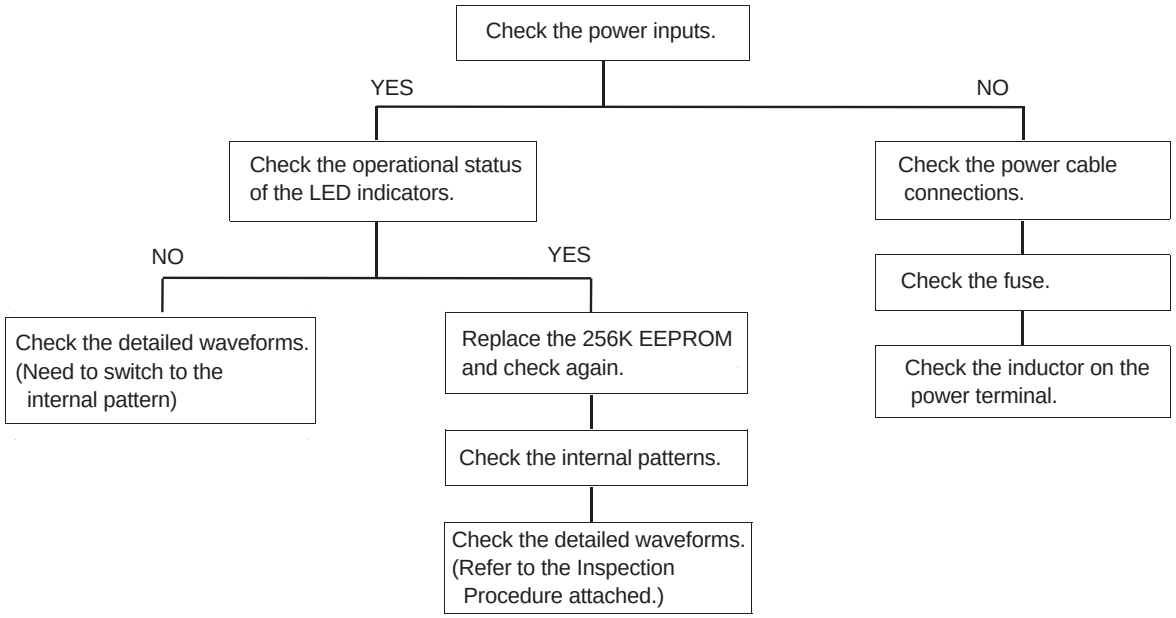
5-5-2 Waveform in Normal Operation

When the PDP set and the logic board operate normally, the operation status LED indicator shown in Figure 1 blinks once per second.
If the set has a problem, visually check the LED status and replace the board if any error is found. If you need to detect and check errors, follow the directions given in the Attachment: “Logic Board Inspection Procedure”.

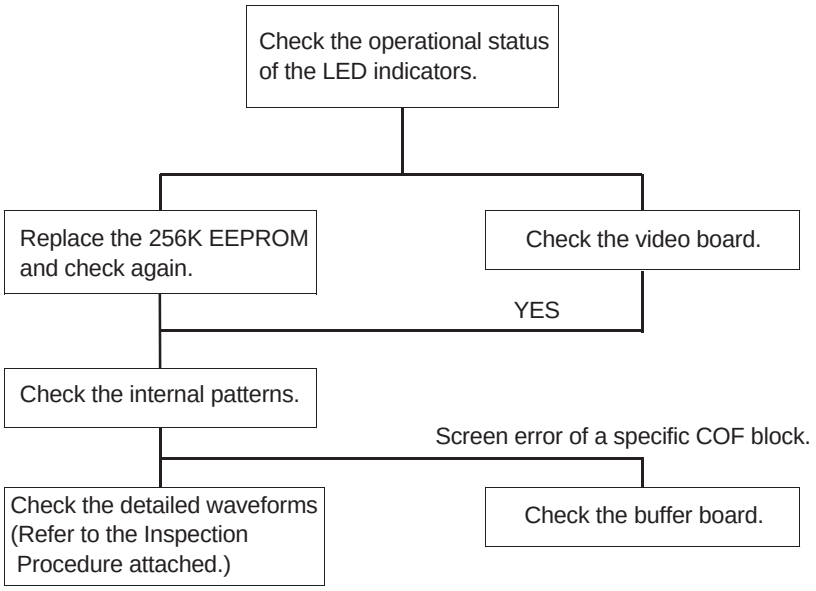
5-5-3 Troubleshooting

There are several reasons an error can occur on to the logic board. The following flow charts show solutions to many problems.

5-5-3(A) No Screen Display Output



5-5-3(B) Screen Error



♦ Terminology

1. 42” SD S2.0 Logic Main Board
 1-1 Main Board
  Applies video signals to the PDP by signaling to the X and Y drive boards and the logic E, F, and G buffers.

2. 5V, 3.3V
 2-1 5V : Voltage that passes through the logic main board and is applied to the logic buffer.
 2-2 3.3V : Main power that is supplied to the logic main board.

♦ Preparations for Inspection

1. Testing the device/instrument: Measurement instruments should be used to finish calibration.
 1-1 Inspection Table: Should supply both 110V and 220V power. It should have sufficient space to accom modate all measurement instruments and samples.
 1-2 Oscilloscope: Should have more than 2 channels. The frequency should be 500MHz.
 1-3 Power Supply: One linear power supply that has the capacity for more than 5V/3A should be prepared for supplying the main power. It should have a current limit function so that it can prevent over current due to abnormal operation of the samples.
 1-4 Logic Main Board: Perform testing on an inspection target board with TEST PROM.

2. Additionally, prepare needed measuring tools such as Vernier calipers and a multimeter.

♦ Preparations for Inspection

1. Inspection Method & Procedure and Acceptance Determination
2. Sample Status: The package of samples should arrive covered when delivered directly from the manufacturer.
3. Inspection Items: On the Inspection Record Sheet record the measurement results of the waveforms specified on Attachment 1 : TEST POINT.
4. Inspection Procedure
 4-1 Inspect the width and length of the logic buffer board by using Vernier calipers, which have been calibrated. Determine compliance to the specifications by referring to the numbers and drawings below. Record the inspection result on the Inspection Record Sheet.
 4-2 Inspect the type, location and installation orientation of the connectors and record the results on the Inspection Record Sheet.
 4-3 Visually inspect the soldering state of the ASS’Y Y. First, inspect the omitted part slots on the mounting surface and the short-circuits on the various ICS and connector pins, and then inspect the short-circuits on th opposite side. When the visual inspection is finished, record the inspection results on the Inspection Record Sheet.

4-4 Board Drawings and Appearance

1) Logic Main Board

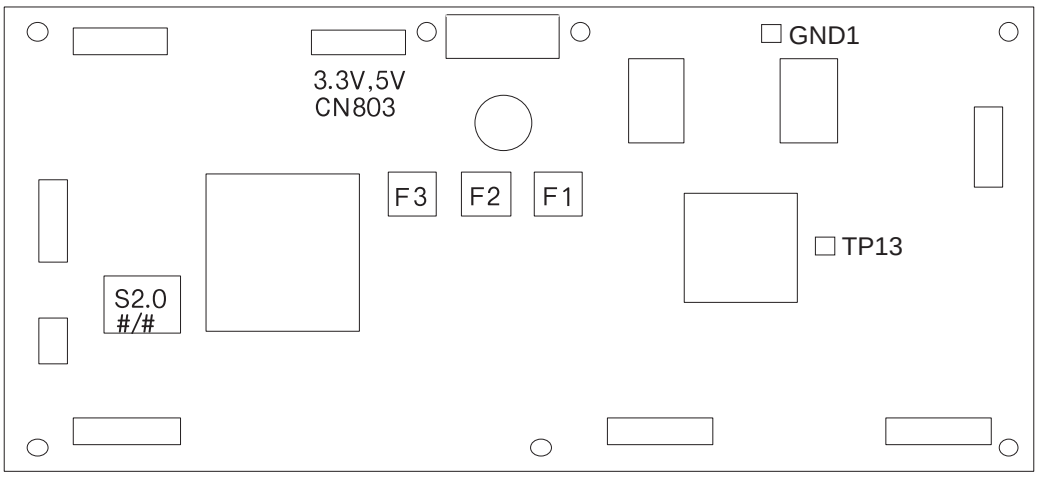


Figure 1. Appearance of the Logic Main Board

4-5 Logic Main Board Switch Operation

1) Internal Pattern: Set SW2001 No.2, and 4 to OFF(DOWN), No.3 to ON(UP).
2) External Pattern: Set SW2001 No.2, and 4 to ON(UP), No.3 to OFF(DOWN)/
❊ Manipulate the switches to the internal pattern for board inspection.
❊ Ignore SW201 No.1.

4-6 Board Inspections

1) All logic main boards should be completely inspected.
2) Visually inspect the part-soldering state of the entire board.
3) Set the instruments for waveform inspection.
① When a linear power supply is used, set the output voltages to 5V or 3.3V in advance. When a SMPS is used, ensure that the output voltages are 5V or 3.3V.
② Set the oscilloscope to 4ms/div and 2V/div.
Connect PROBE 1 as shown in the following figure and set it to TRIGGER.
Perform the test by capturing the waveforms from each point with PROBE 2.

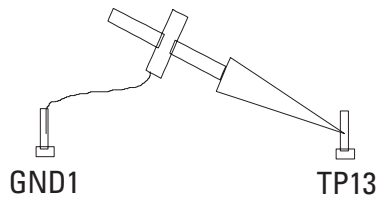


Figure 2. Connecting probe 1 of the oscilloscope

4) Perform waveform inspection

Inspection: Inspect each board separately.

① Place the logic main boards on the inspection table so that they do not touch each other.
❊ Install the TEST PROM and check the SW2001 setting.

② Connect CN803 of the logic main board to the linear power supply (or SMPS).
(Use a 10-pin connector cable.)
❊ Make sure to connect when the linear power supply (or SMPS) turned off.

③ Turn on the linear power supply and apply 5V and 3.3V power to the logic main board.
Then, check whether the LD2001 LED indicator, located at the top left of the board, blinks about once per second.
If the LED indicator blinks too fast or is not lit up, it indicates tat the logic board is not operating normally.

④ Measure each waveform on the board and compare to the waveforms on Attachment 1.

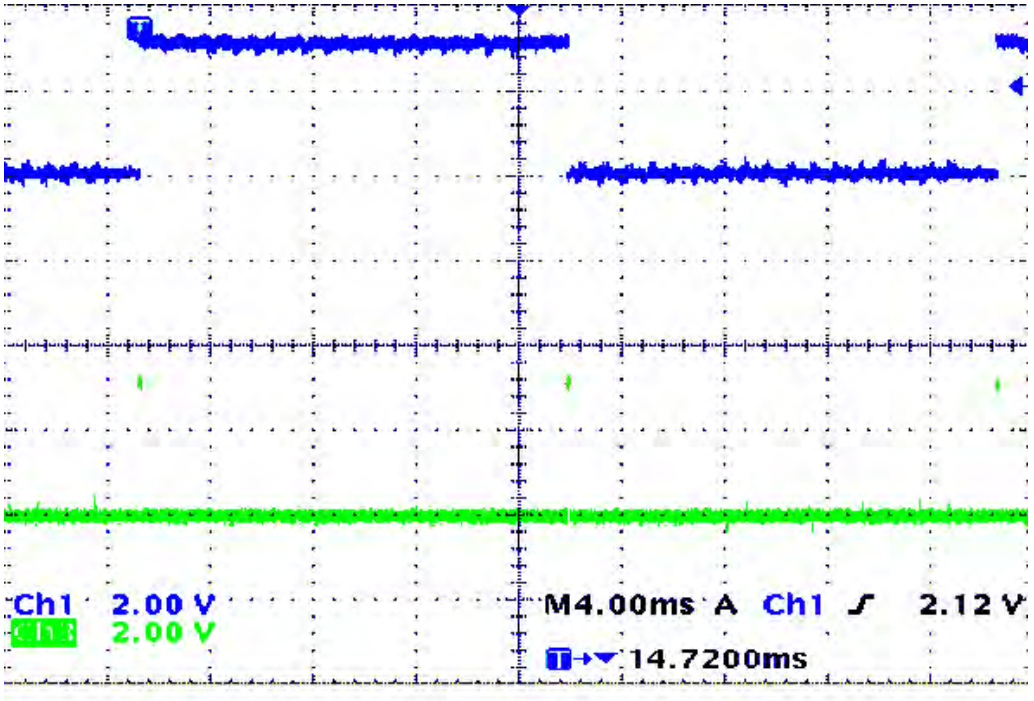
⑤ Finish the inspection and turn the linear power supply (or SMPS) off.

⑥ After completing the inspection, set the SW2001 switch to the external pattern.

5-5-4 SD S2.0 Logic Board Waveforms

❉ Oscilloscope settings: 4.0ms / div, 2V / div

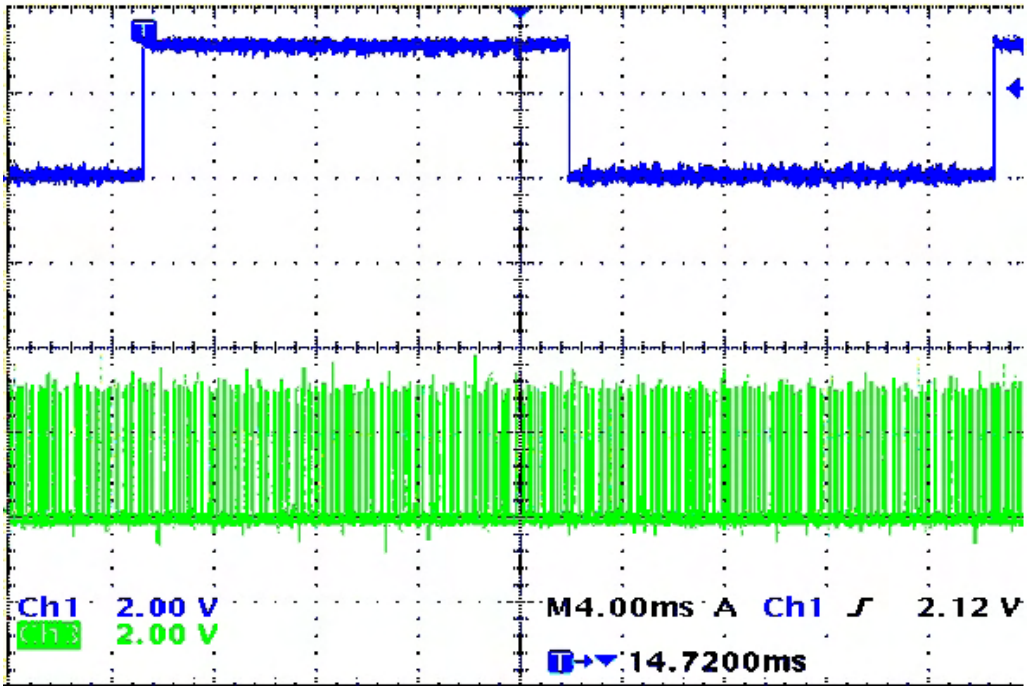
1



signal for trigger
(TP13)
peak to peak
level:3.3V

TP04,VSYNC
peak to peak
level:3.3V
Frequency:60Hz

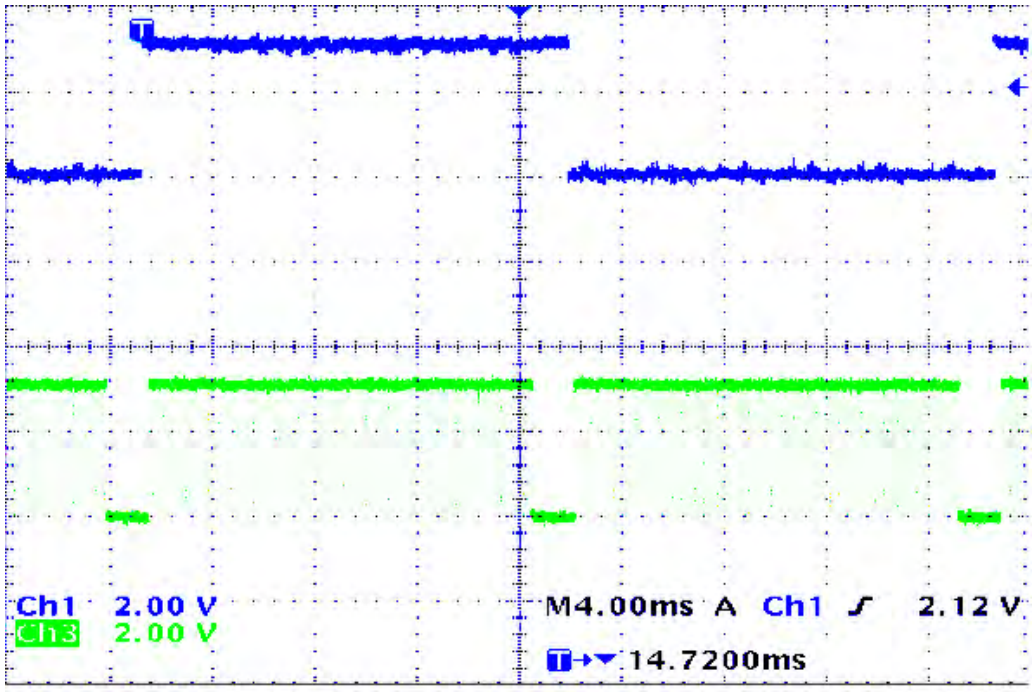
2



signal for trigger
(TP13)
peak to peak
level:3.3V

TP05,HSYNC
peak to peak
level:3.3V

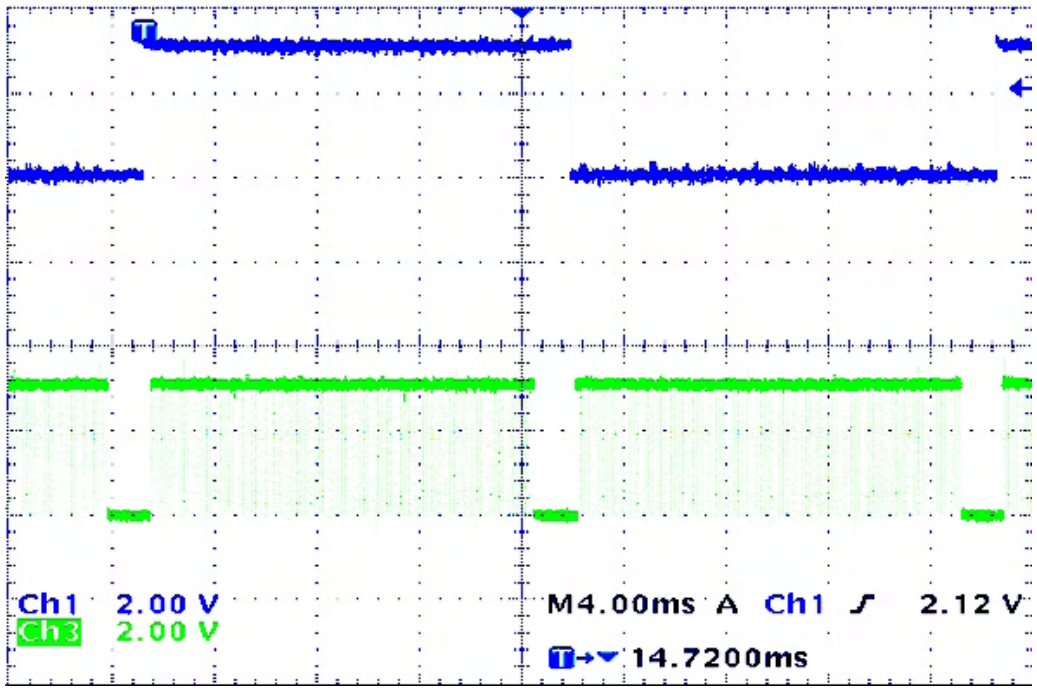
3



signal for trigger
(TP13)
peak to peak
level:3.3V

CN101(6),DATAEN
peak to peak
level:3.3V

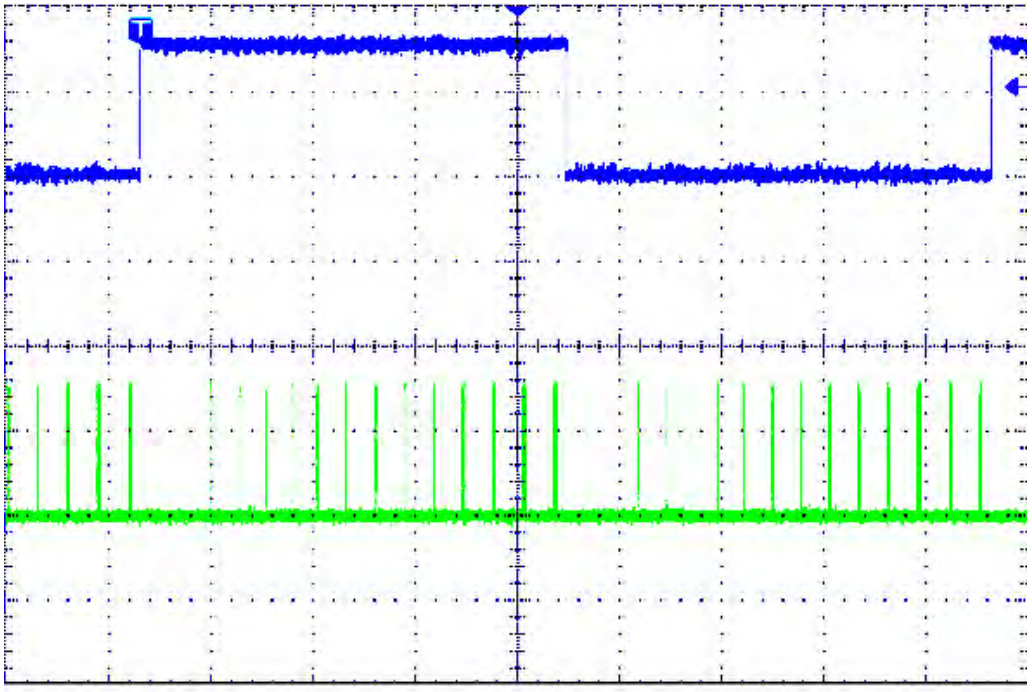
4



signal for trigger
(TP13)
peak to peak
level:3.3V

AR2042~AR2047
Terminal DATA
peak to peak
level:3.3V

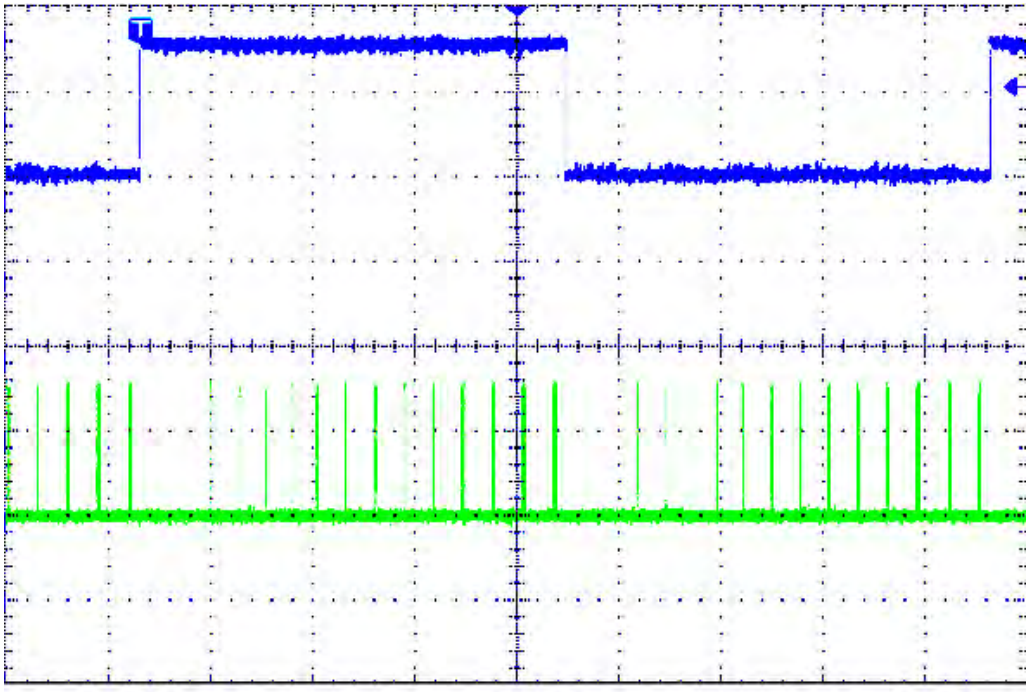
5



signal for trigger
(TP13)
peak to peak
level:3.3V

CN101(6),Xf
peak to peak
level:3.3V

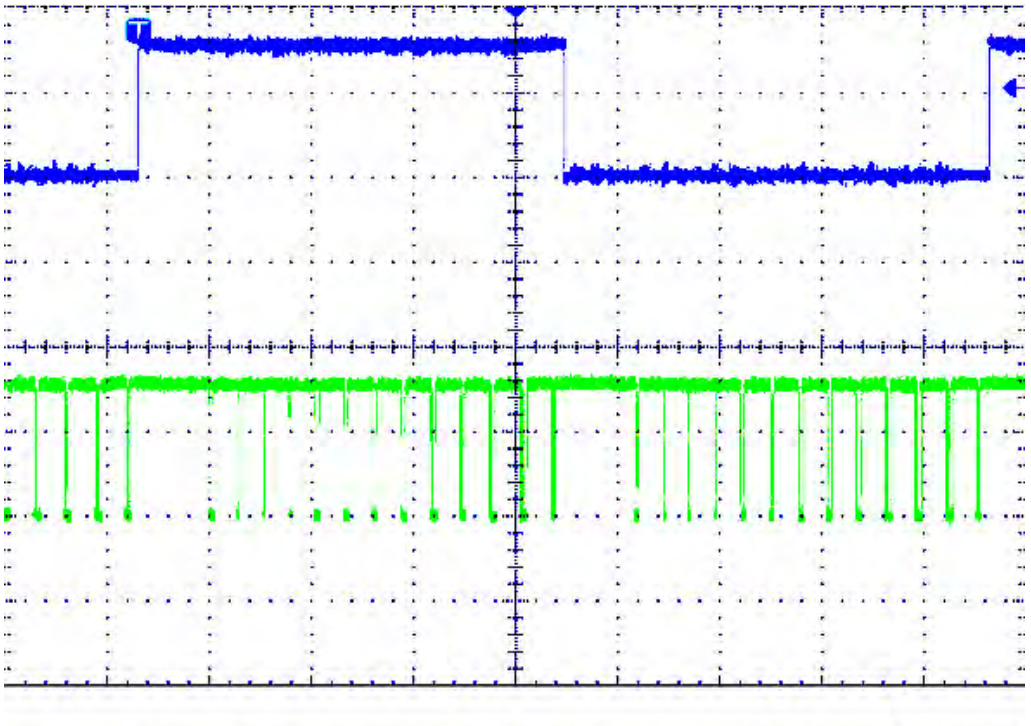
6



signal for trigger
(TP13)
peak to peak
level:3.3V

CN101(8),Xr
peak to peak
level:3.3V

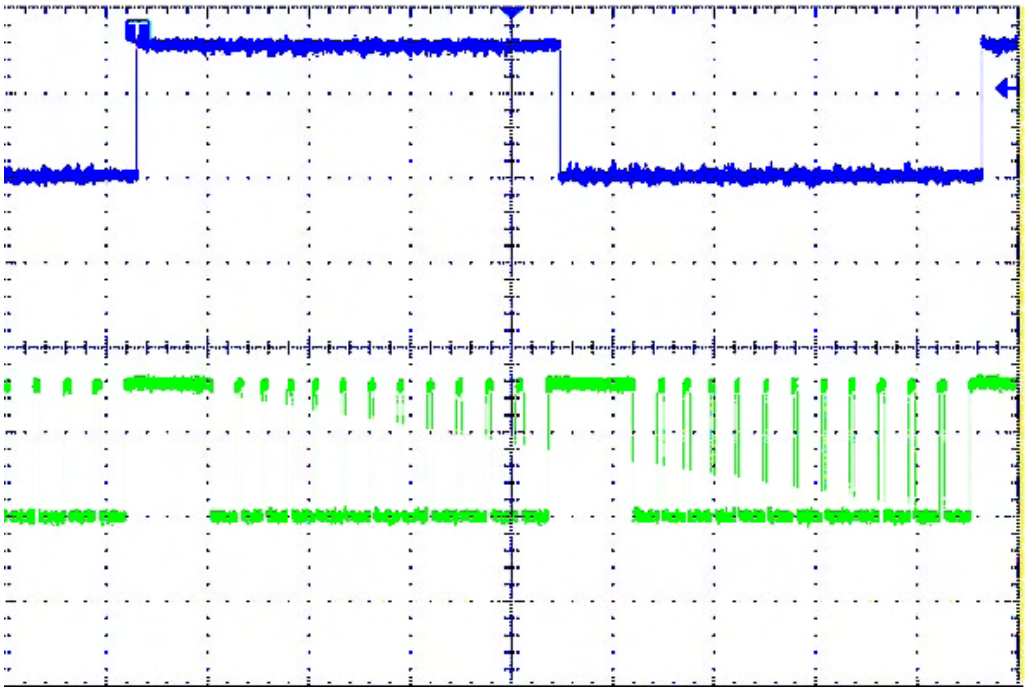
7



signal for trigger
(TP13)
peak to peak
level:3.3V

CN101(10),Xc
peak to peak
level:3.3V

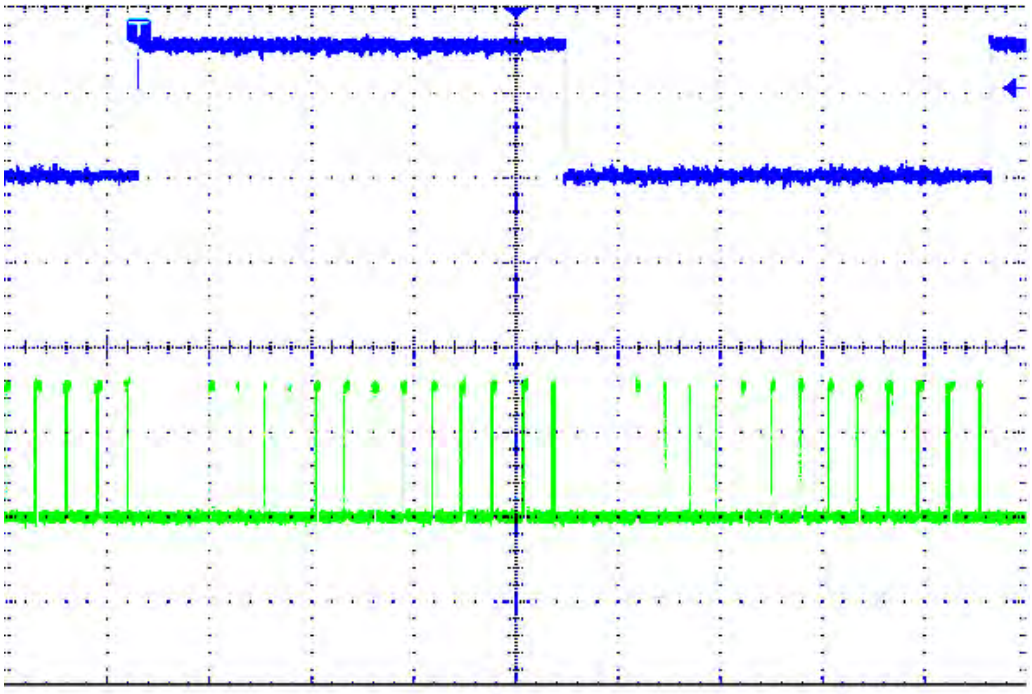
8



signal for trigger
(TP13)
peak to peak
level:3.3V

CN101(12),Xp
peak to peak
level:3.3V

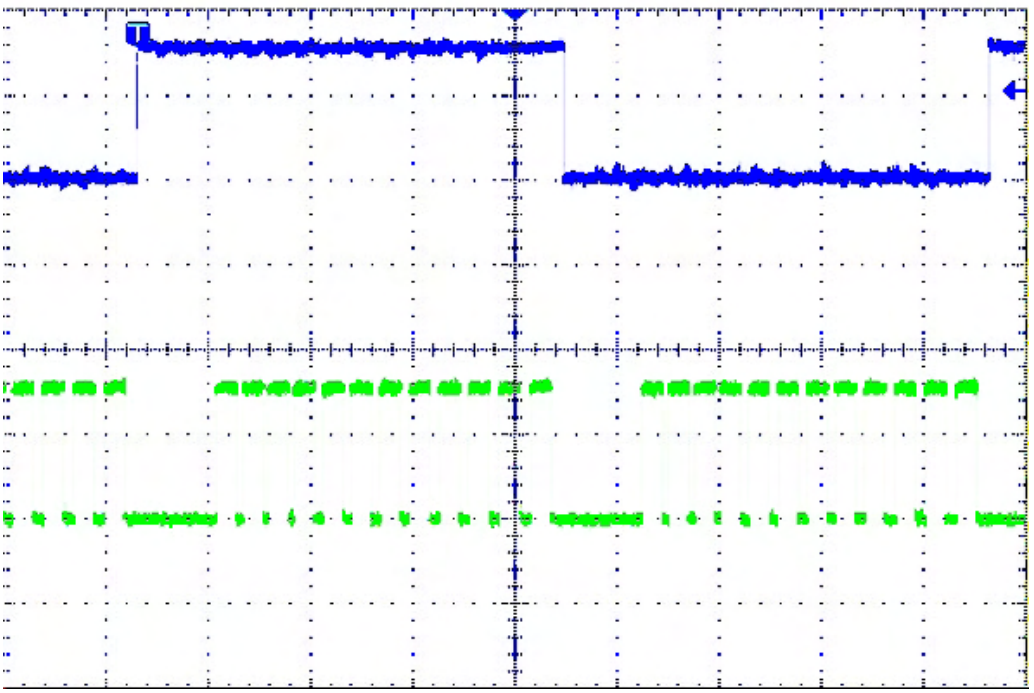
9



signal for trigger
(TP13)
peak to peak
level:3.3V

CN101(14),Xg
peak to peak
level:3.3V

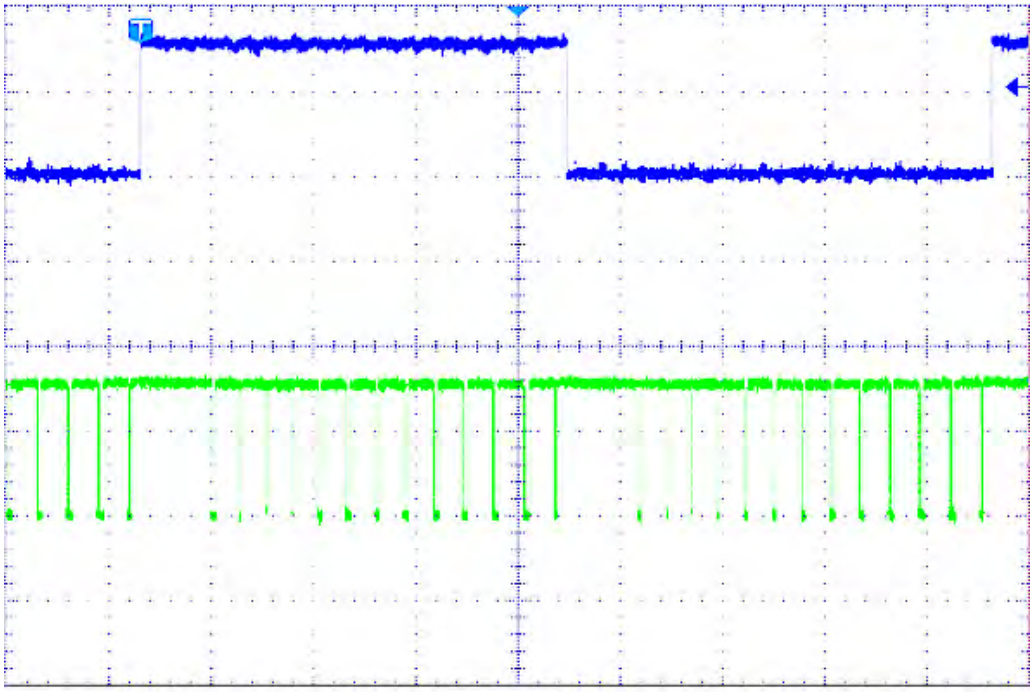
10



signal for trigger
(TP13)
peak to peak
level:3.3V

CN101(16),Xe
peak to peak
level:3.3V

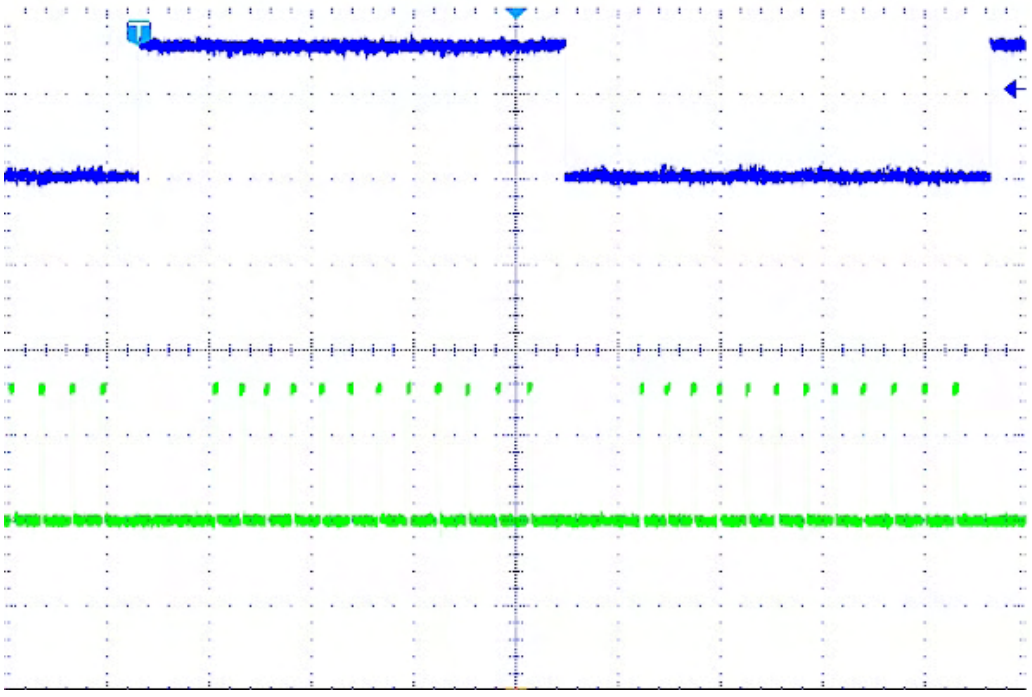
11



signal for trigger
(TP13)
peak to peak
level:3.3V

CN121(8),Xs
peak to peak
level:3.3V

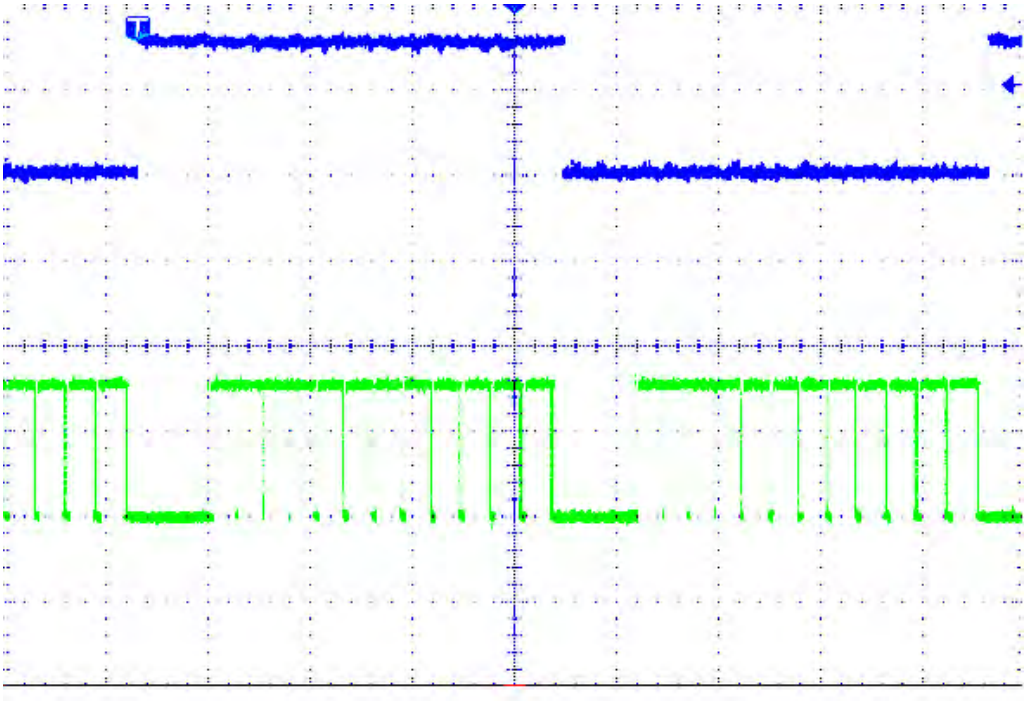
12



signal for trigger
(TP13)
peak to peak
level:3.3V

CN201(4),Yfr
peak to peak
level:3.3V

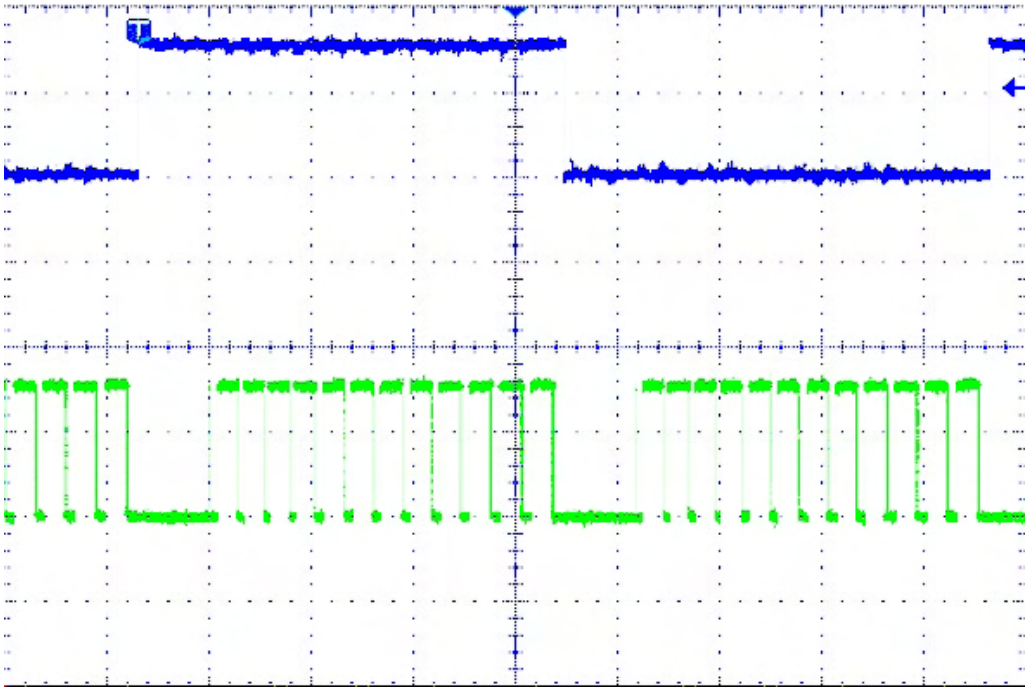
13



signal for trigger
(TP13)
peak to peak
level:3.3V

CN201(6),Yg
peak to peak
level:3.3V

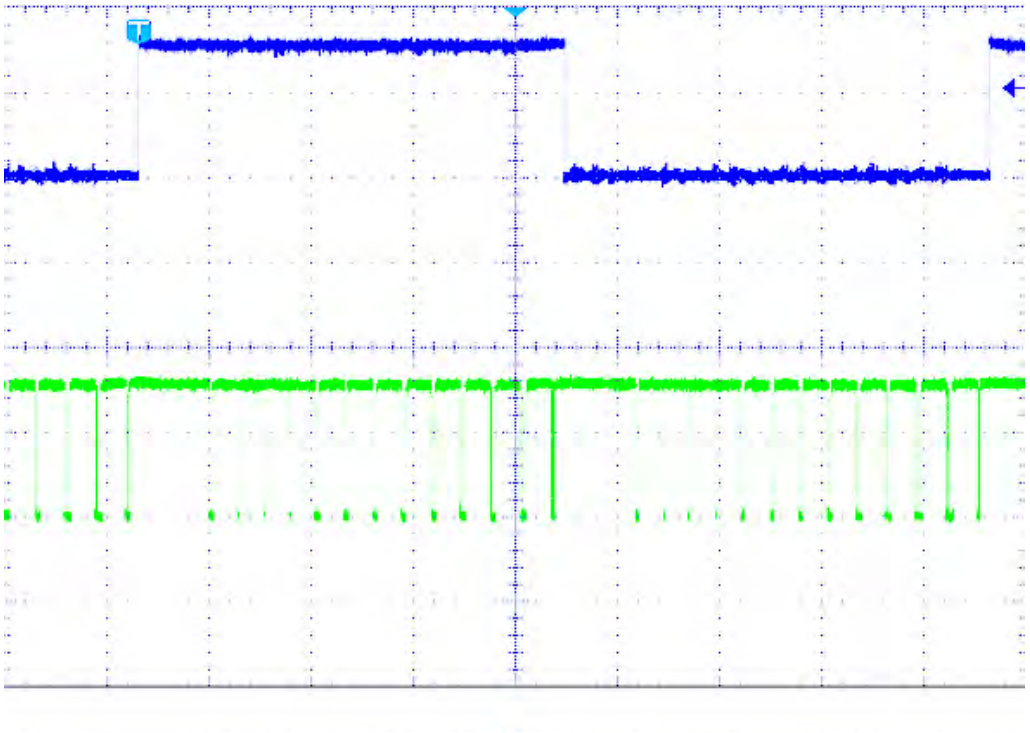
14



signal for trigger
(TP13)
peak to peak
level:3.3V

CN201(8),Y1
peak to peak
level:3.3V

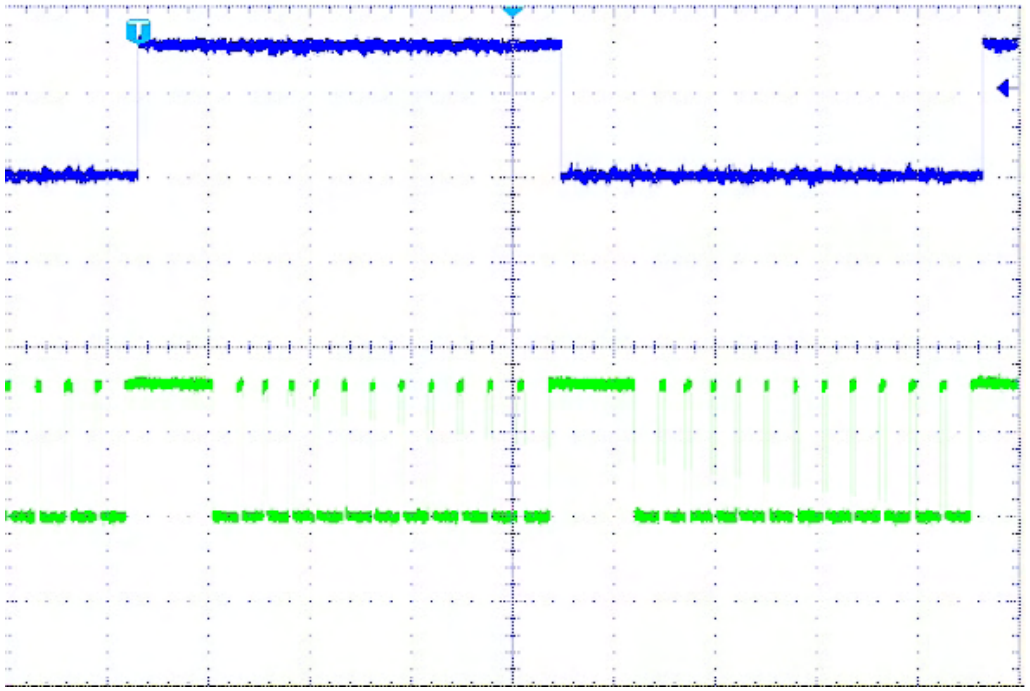
15



signal for trigger
(TP13)
peak to peak
level:3.3V

CN201(10),Yrr
peak to peak
level:3.3V

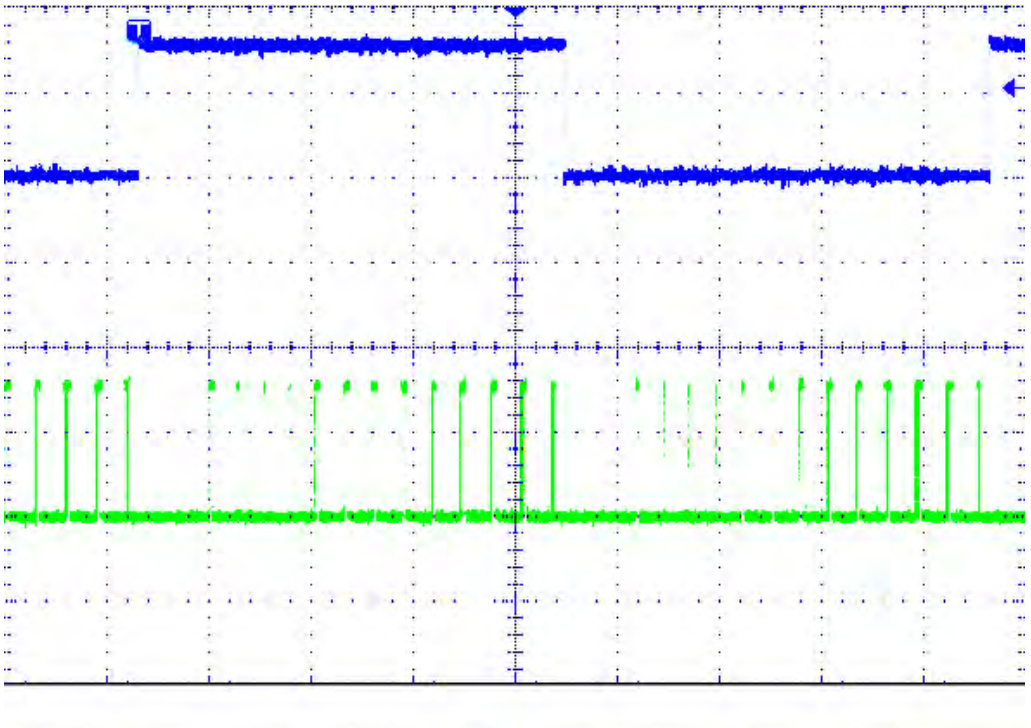
16



signal for trigger
(TP13)
peak to peak
level:3.3V

CN201(12),Ys
peak to peak
level:3.3V

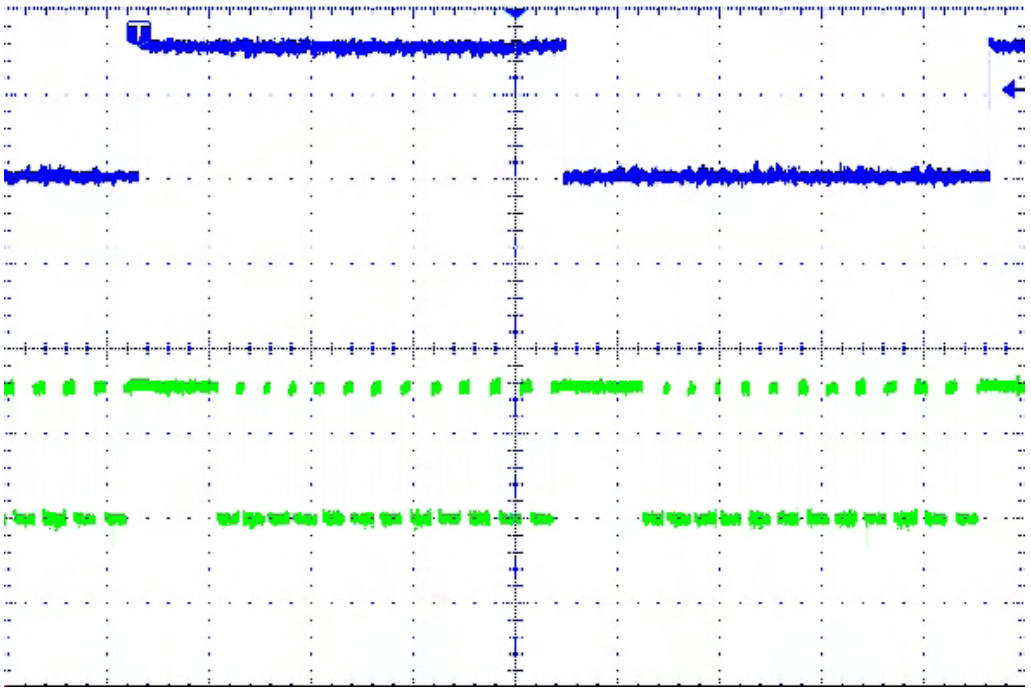
17



signal for trigger
(TP13)
peak to peak
level:3.3V

CN201(14),Yp
peak to peak
level:3.3V

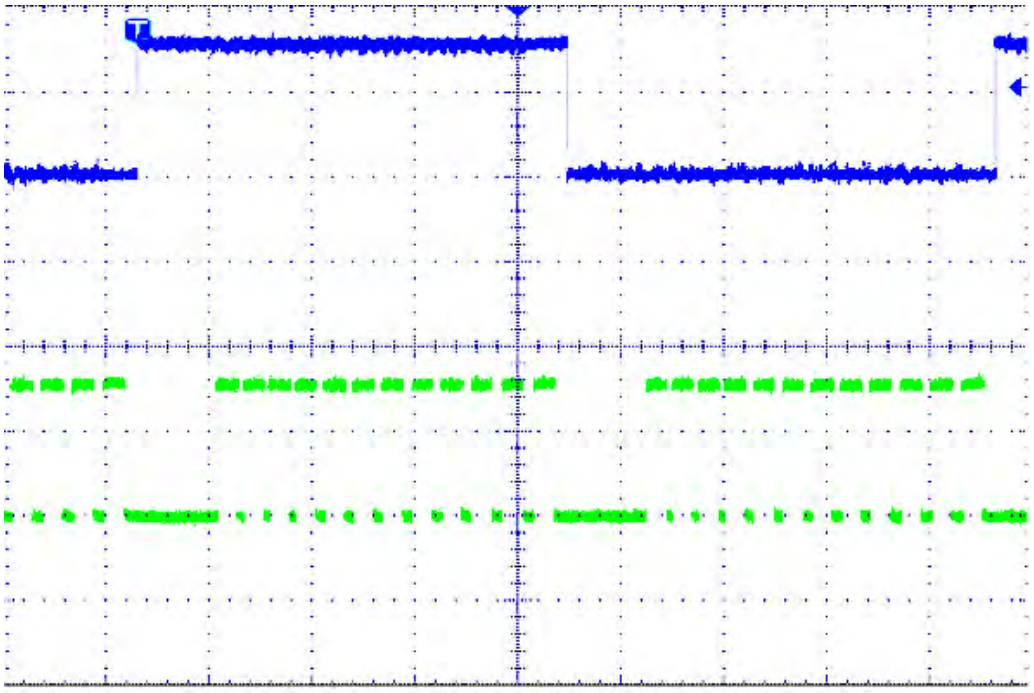
18



signal for trigger
(TP13)
peak to peak
level:3.3V

CN201(6),Ysp
peak to peak
level:3.3V

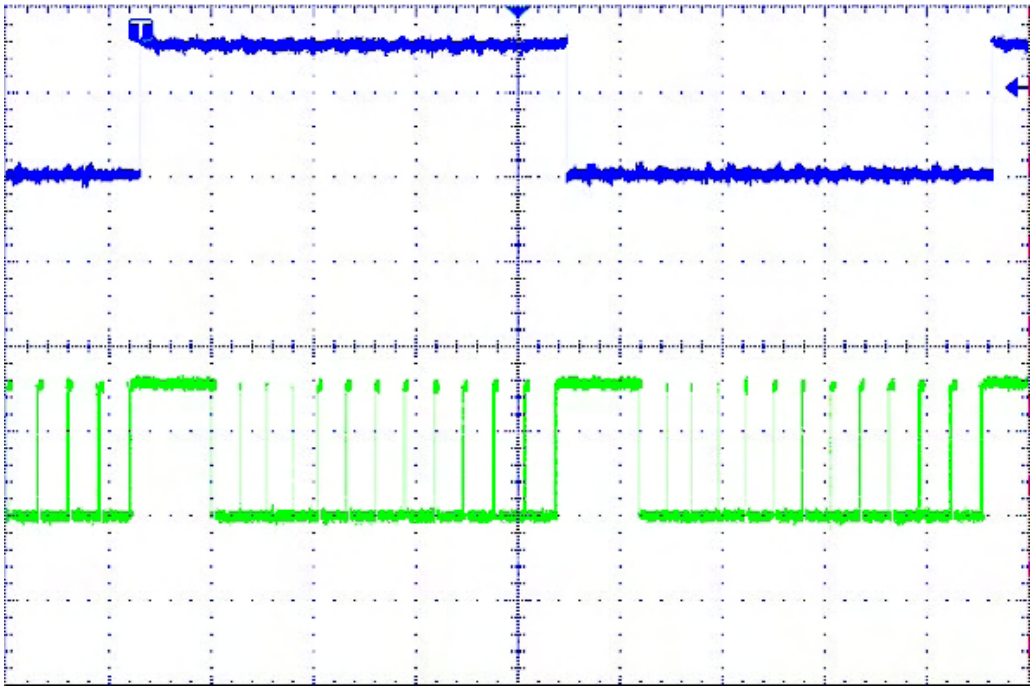
19



signal for trigger
(TP13)
peak to peak
level:3.3V

CN201(18),Ysc
peak to peak
level:3.3V

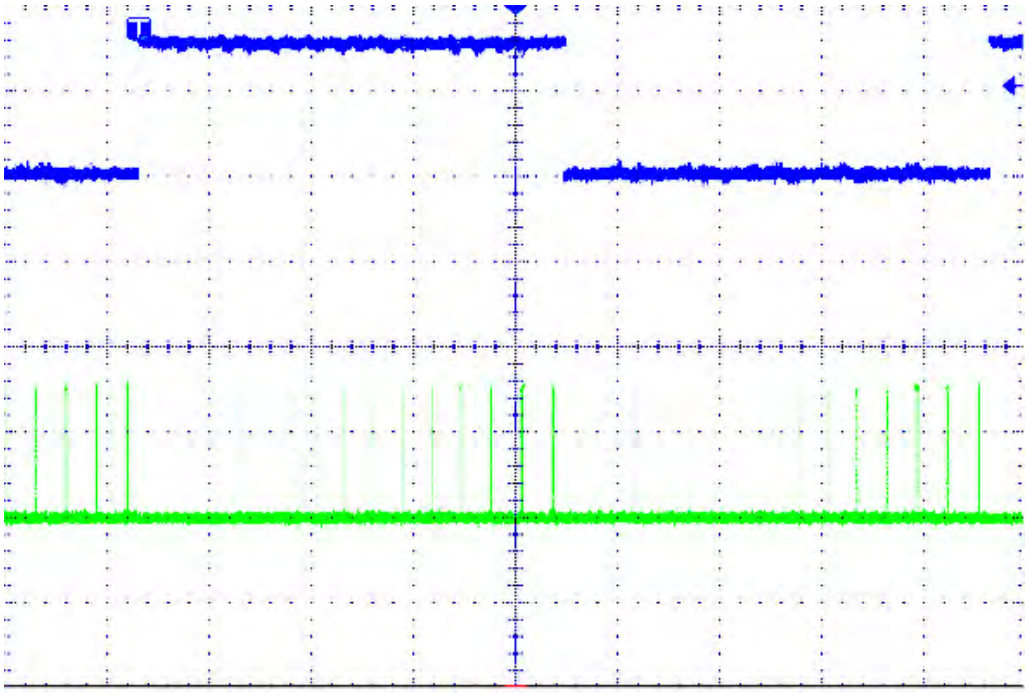
20



signal for trigger
(TP13)
peak to peak
level:3.3V

CN201(20),Yc
peak to peak
level:3.3V

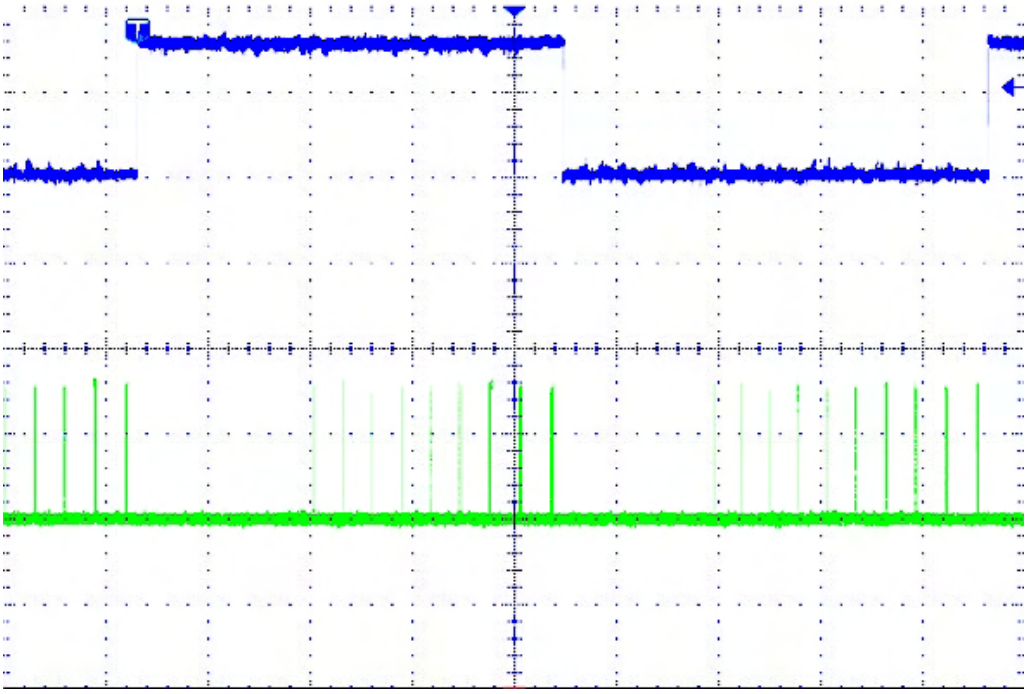
21



signal for trigger
(TP13)
peak to peak
level:3.3V

CN201(22),Yr
peak to peak
level:3.3V

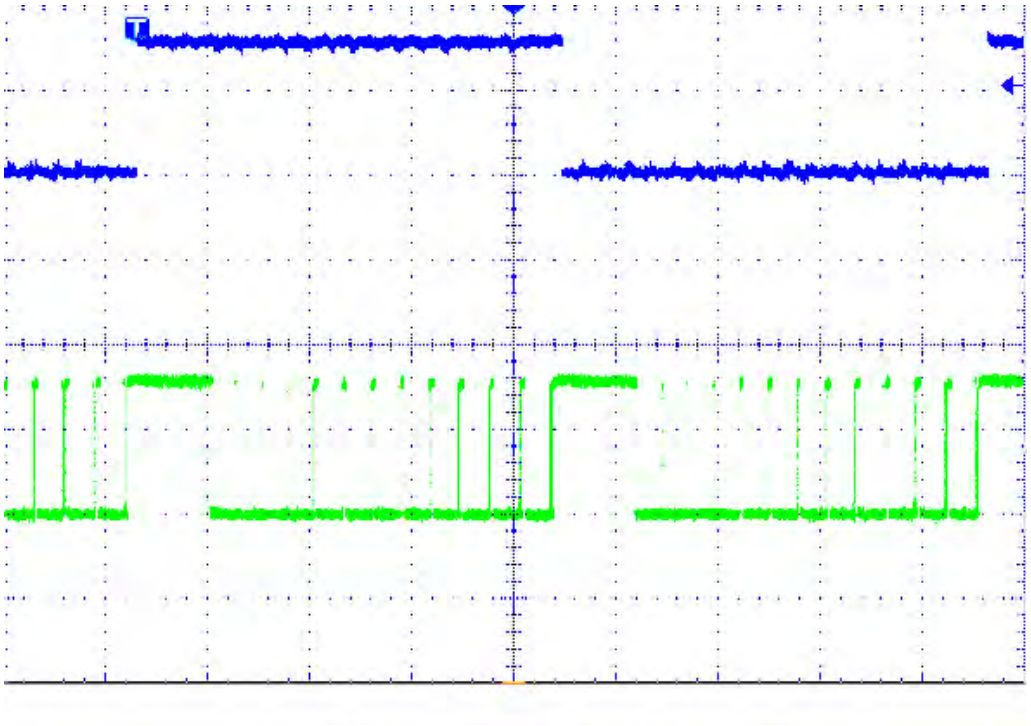
22



signal for trigger
(TP13)
peak to peak
level:3.3V

CN201(24),Yf
peak to peak
level:3.3V

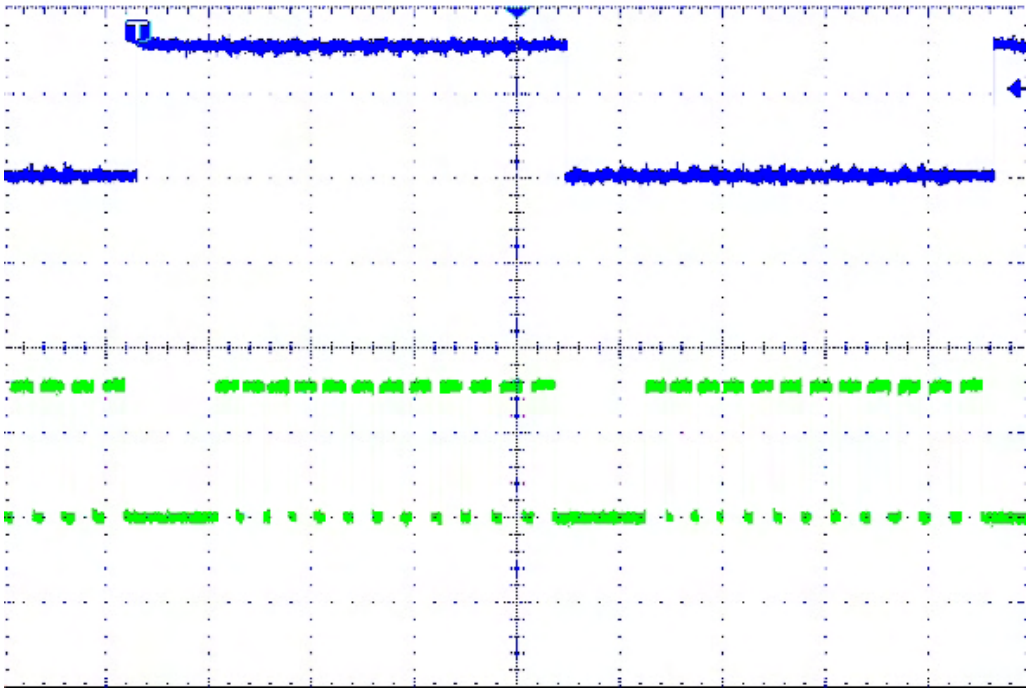
23



signal for trigger
(TP13)
peak to peak
level:3.3V

CN201(26),Ysc_c
peak to peak
level:3.3V

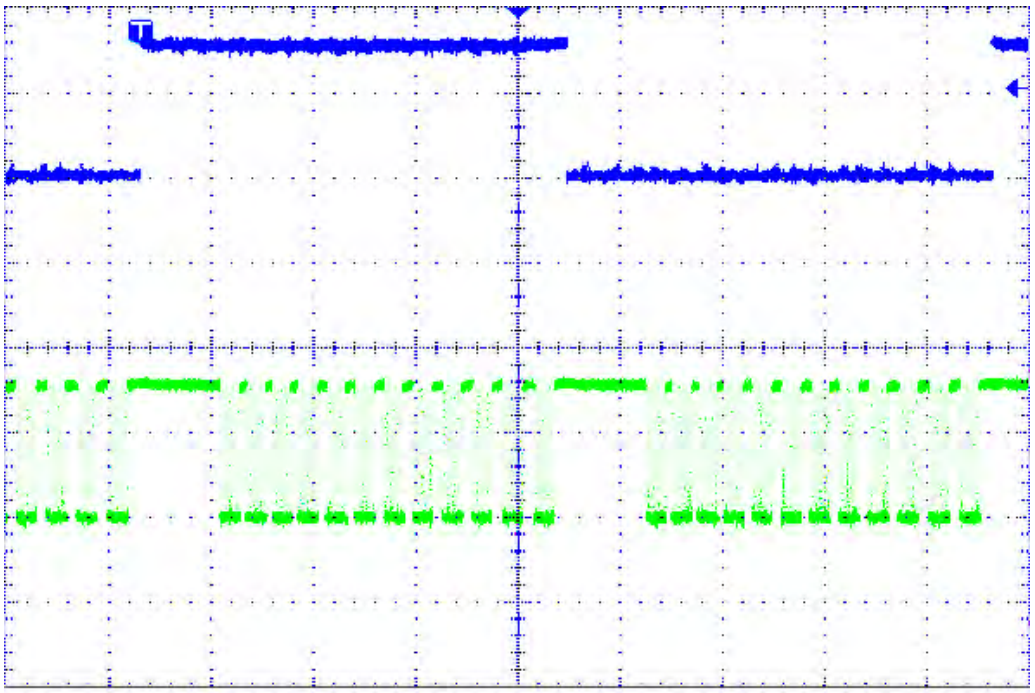
24



signal for trigger
(TP13)
peak to peak
level:3.3V

CN201(30),TSC
peak to peak
level:3.3V

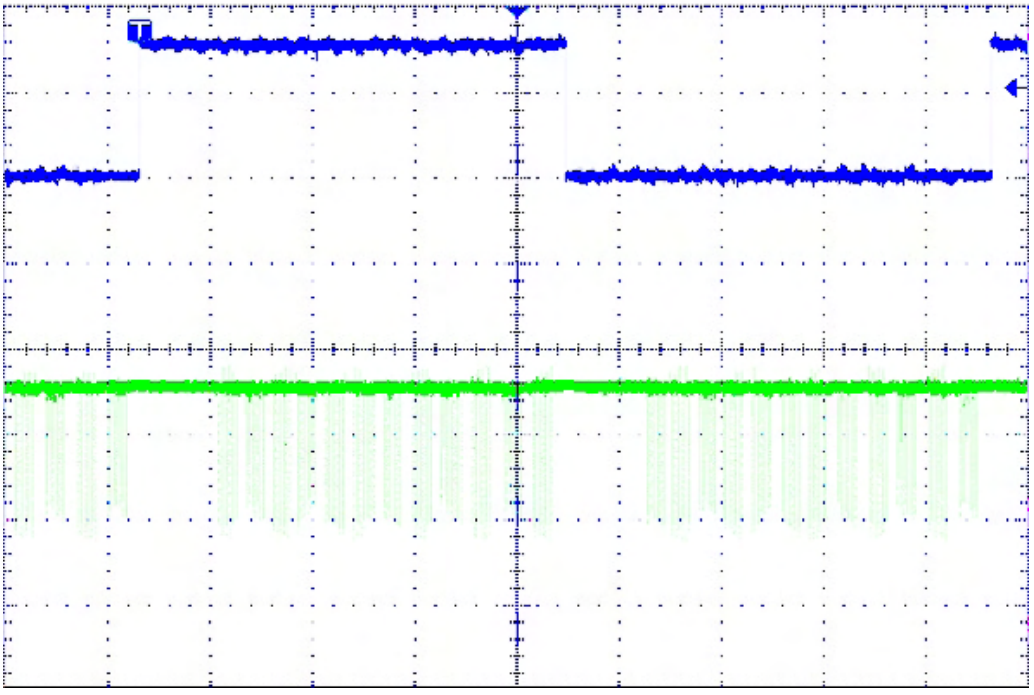
25



signal for trigger
(TP13)
peak to peak
level:3.3V

CN201(32),STB
peak to peak
level:3.3V

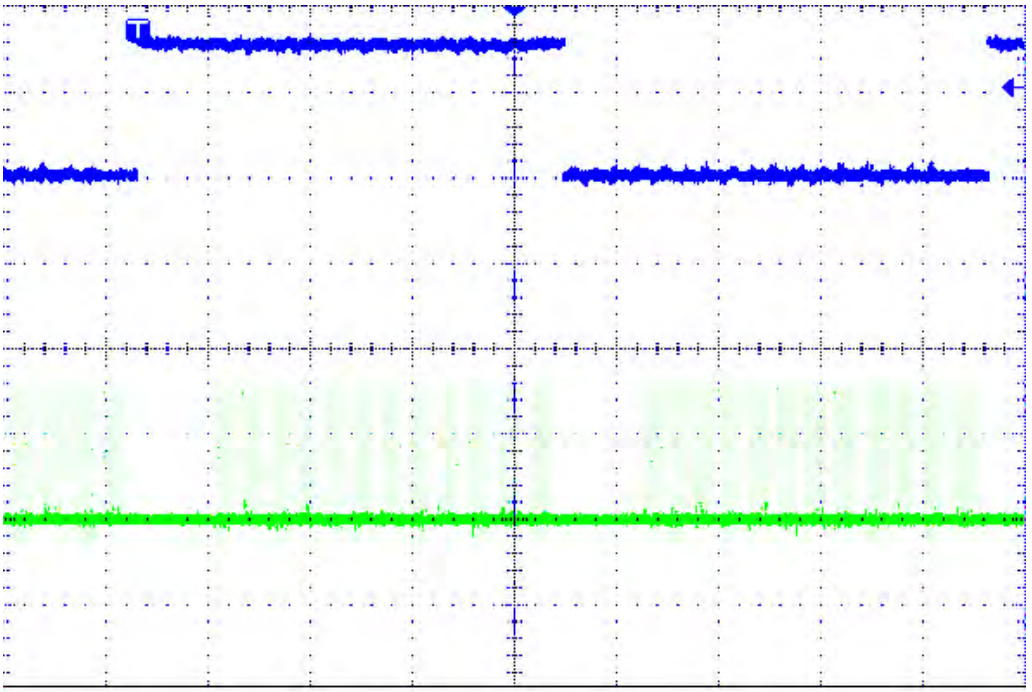
26



signal for trigger
(TP13)
peak to peak
level:3.3V

CN201(34),LE
peak to peak
level:3.3V

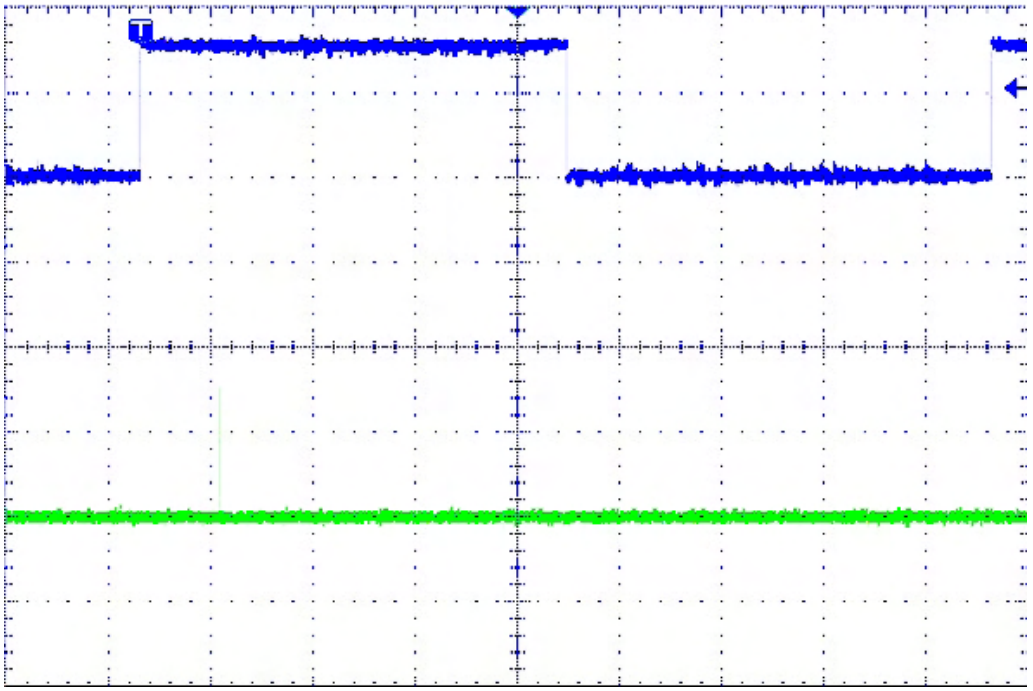
27



signal for trigger
(TP13)
peak to peak
level:3.3V

CN201(36),CLK
peak to peak
level:3.3V

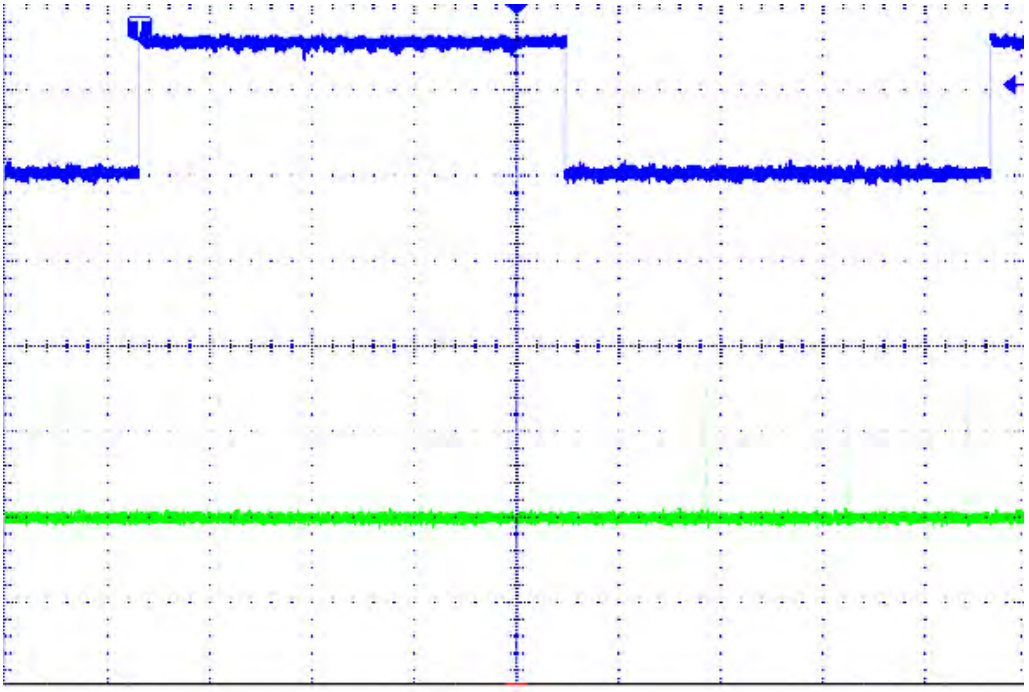
28



signal for trigger
(TP13)
peak to peak
level:3.3V

CN201(38),SIA
peak to peak
level:3.3V

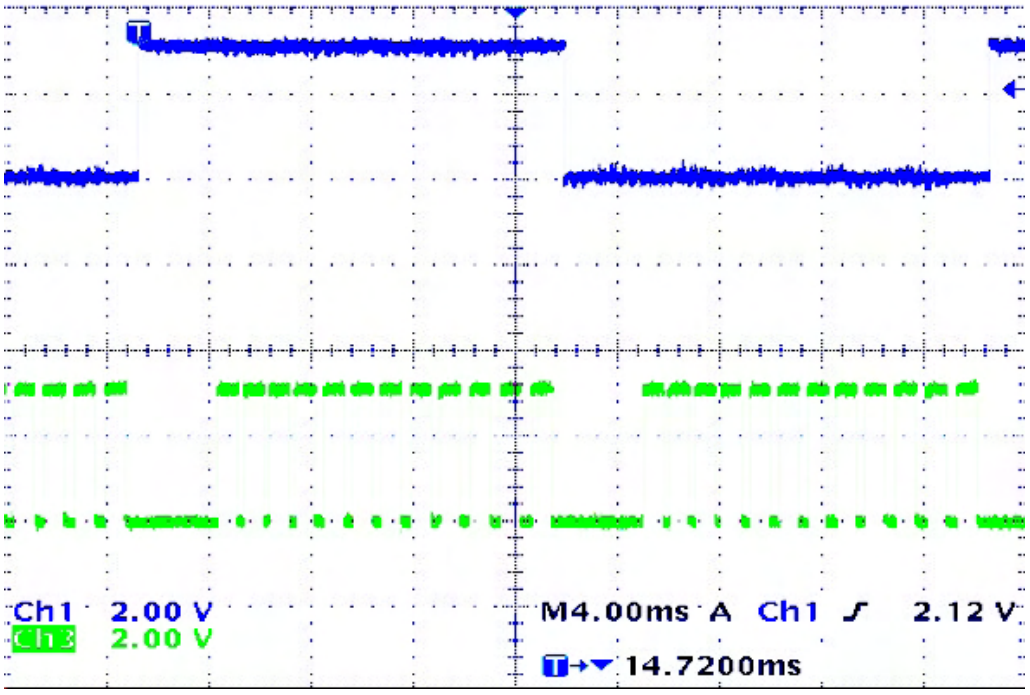
29



signal for trigger
(TP13)
peak to peak
level:3.3V

CN201(40),SIB
peak to peak
level:3.3V

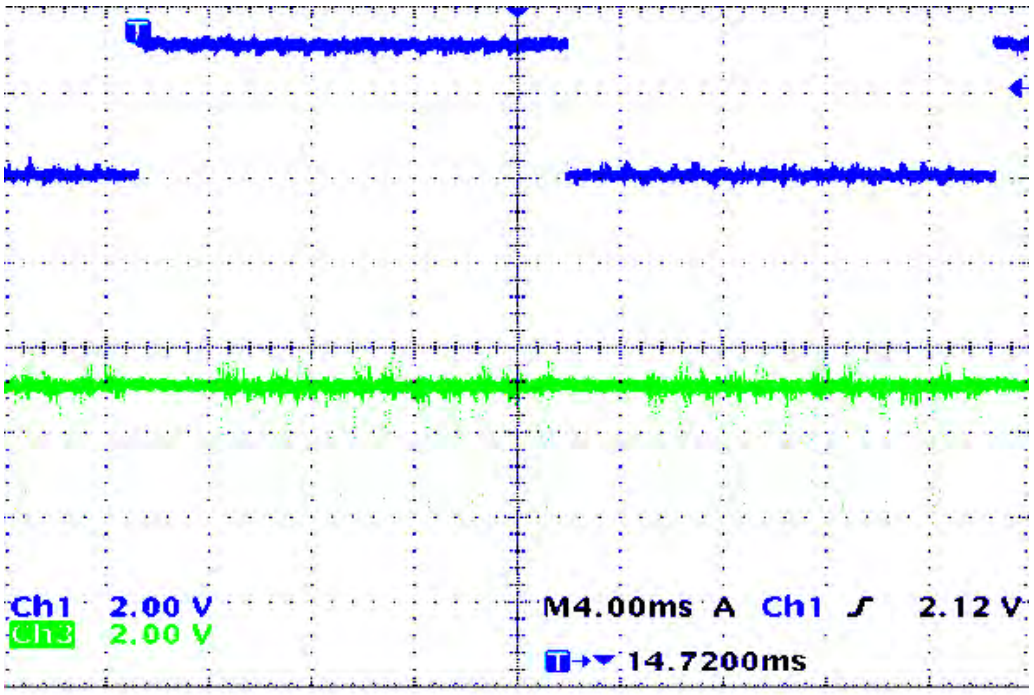
30



signal for trigger
(TP13)
peak to peak
level:3.3V

AR2009(1,2,3),POL
peak to peak
level:3.3V

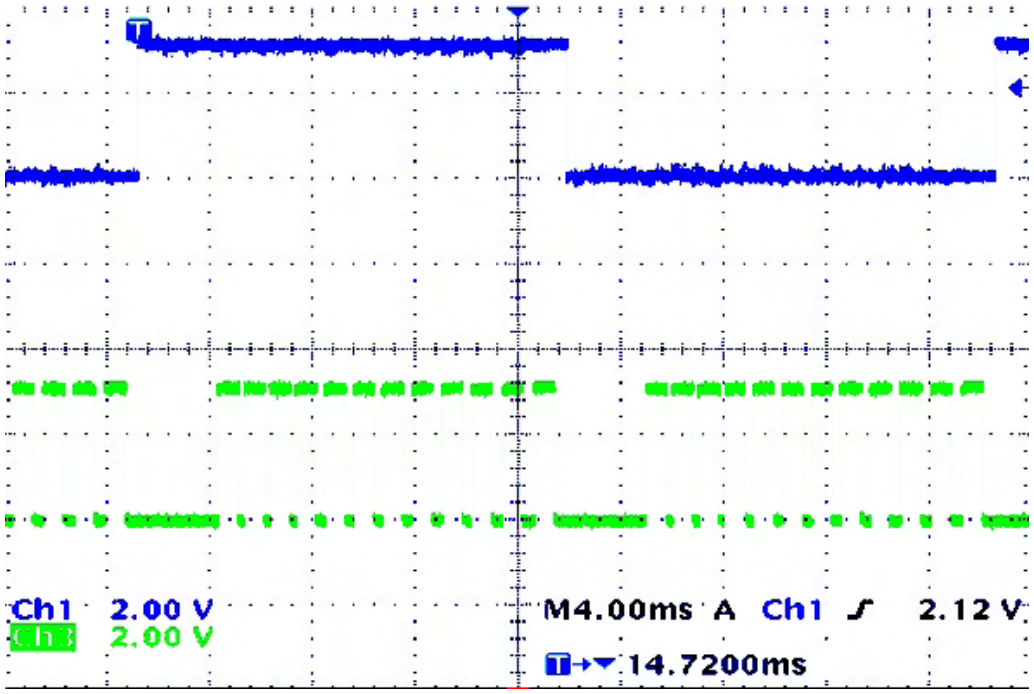
31



signal for trigger
(TP13)
peak to peak
level:3.3V

AR2009(4),
AR2008(1,2),STB
peak to peak
level:3.3V

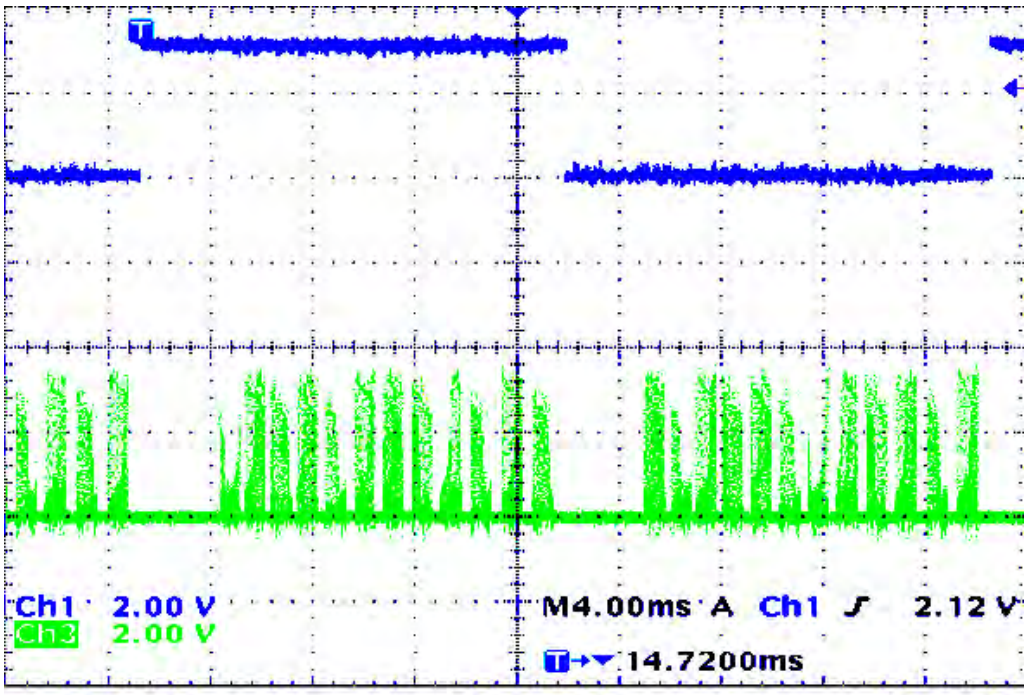
32



signal for trigger
(TP13)
peak to peak
level:3.3V

AR2010(2,3,4),
BLK
peak to peak
level:3.3V

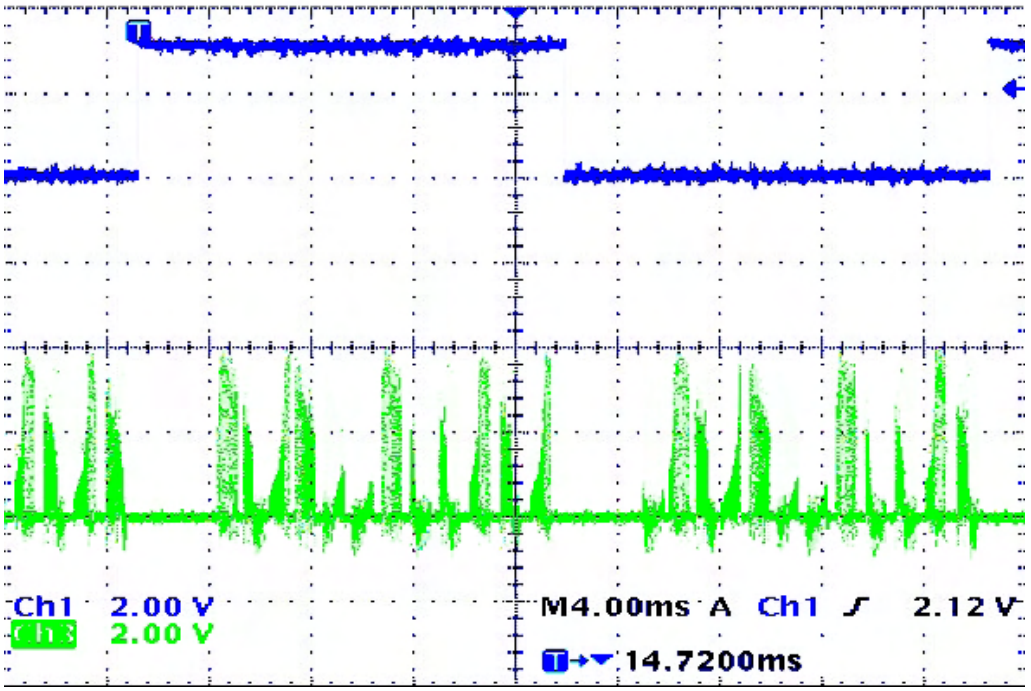
33



signal for trigger
(TP13)
peak to peak
level:3.3V

AR2008(3,4),
AR2007(1),
SCLK_1
peak to peak
level:3.3V
Frequency:20MHz

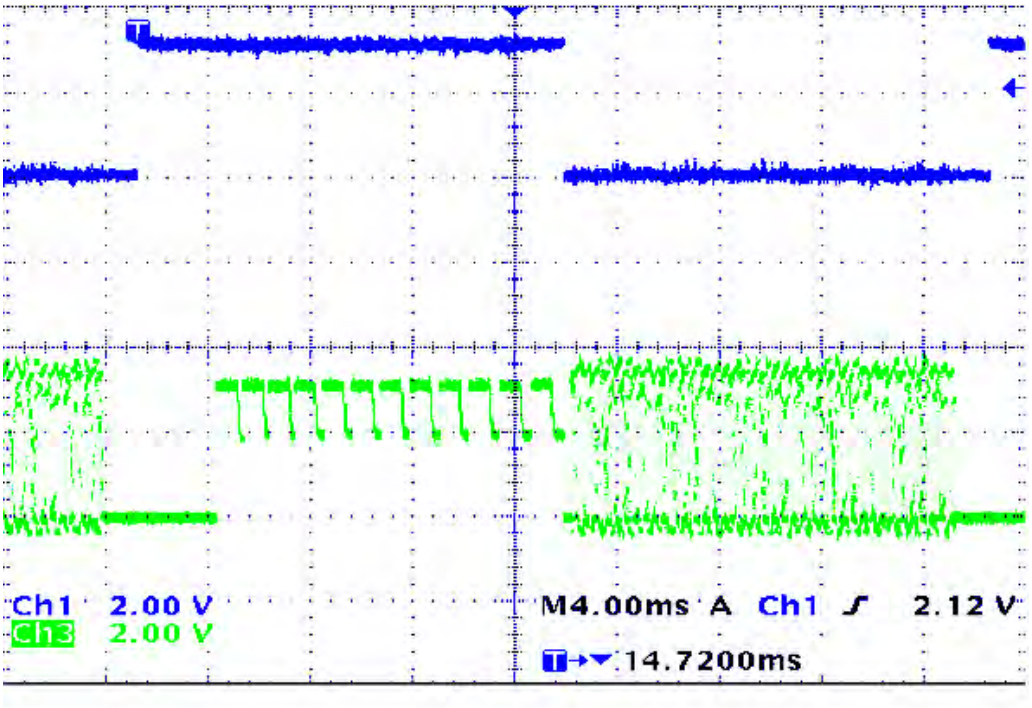
34



signal for trigger
(TP13)
peak to peak
level:3.3V

AR2007(2,3,4),
SCLK_2
peak to peak
level:3.3V
Frequency:20MHz

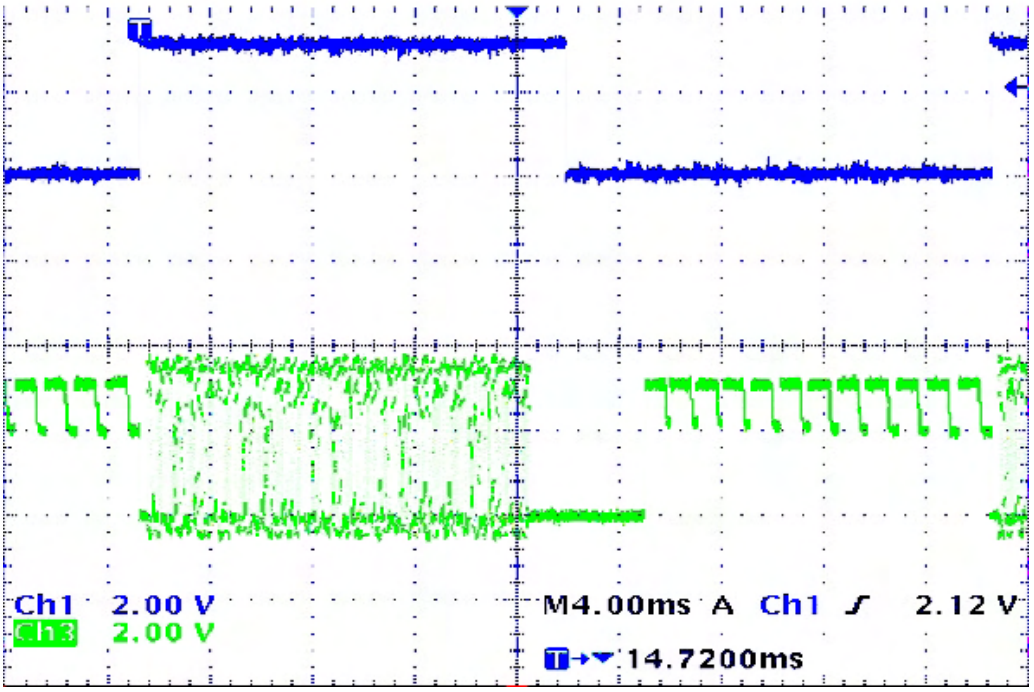
35



signal for trigger
(TP13)
peak to peak
level:3.3V

U2013(2),DATA
peak to peak
level:3.3V

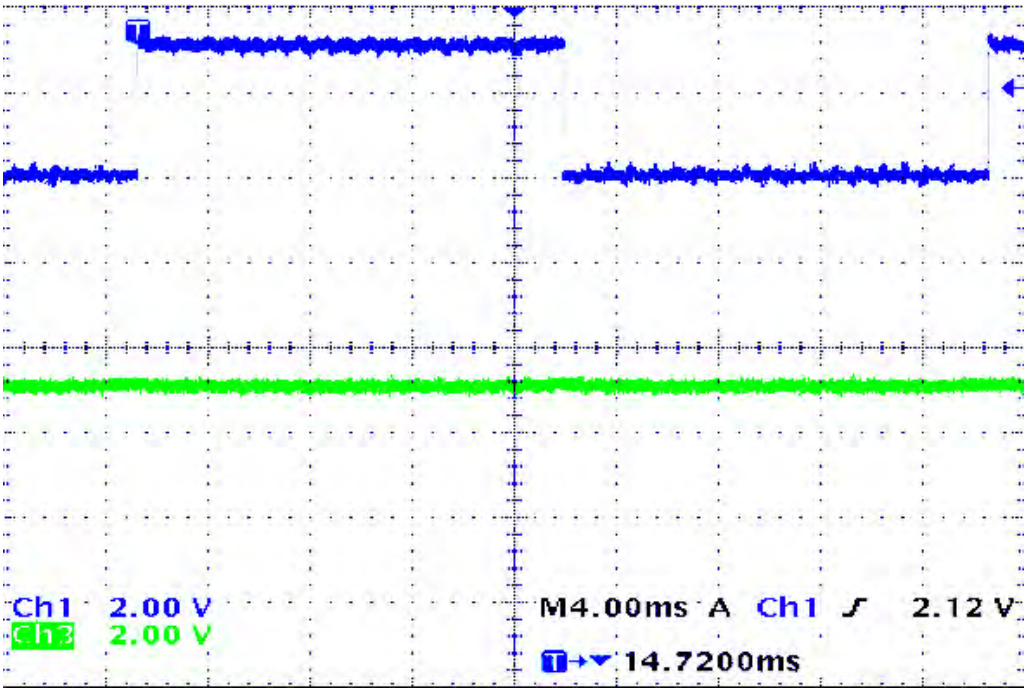
36



signal for trigger
(TP13)
peak to peak
level:3.3V

U2014(2),DATA
peak to peak
level:3.3V

37



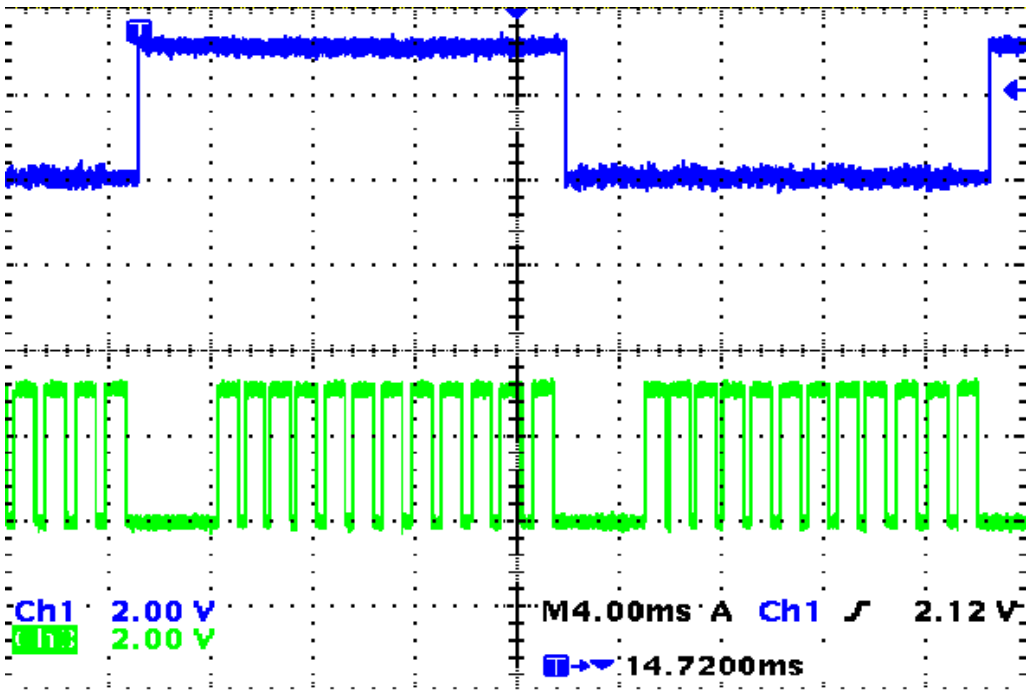
signal for trigger (TP13)
peak to peak level:3.3V

AR2011~AR2034 [Do not inspect the waveforms for AR2012(1), AR2015(1), AR2016(4), AR2017(4), AR2025(1), AR2026(4), AR2031(1), AR2030(4), AR2032(3), AR2033(2), and AR2034(3)]
peak to peak level:3.3V

5-5-5 42" SD S2.0 LOgic Buffer Board Waveforms

❊ Oscilloscope settings: 4.0ms / div, 2V / div
Since the 80-pin connectors have the same pin-outs, the same inspection is applied for all 80-pin connectors. The output voltage of PROBE 2 should be 5V for inspection.

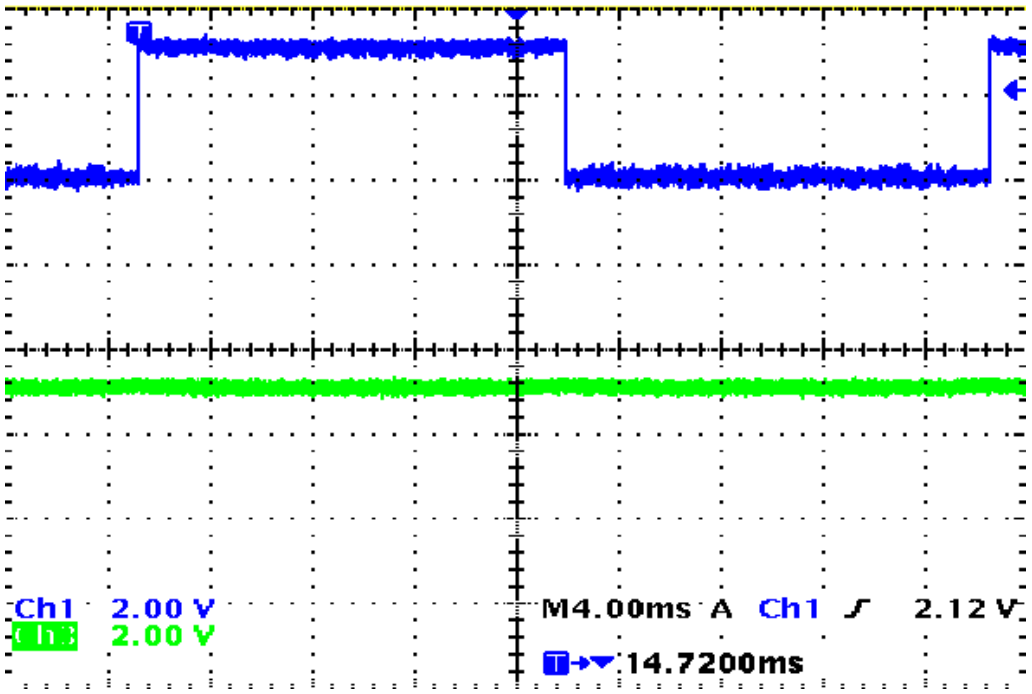
1



signal for trigger (TP13)
peak to peak level:3.3V

EC1,EC2,EC3,FC4, GC5,GC6,GC7(16, 30,54,68),POL
peak to peak level:5V

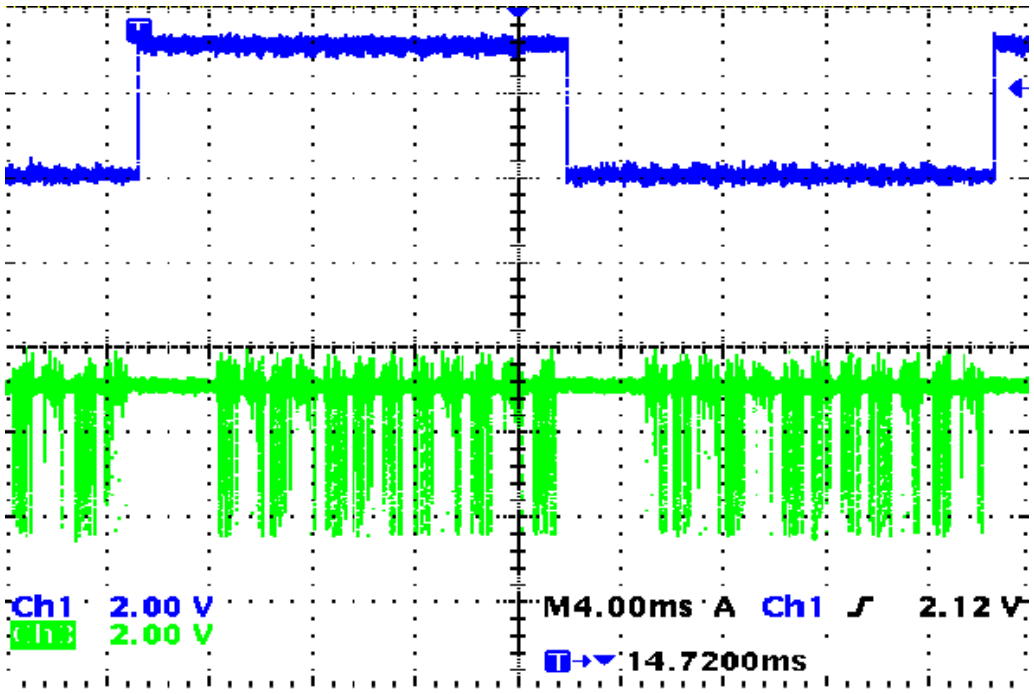
2



signal for trigger (TP13)
peak to peak level:3.3V

EC1,EC2,EC3,FC4, GC5,GC6,GC7(9~ 14,23~28,47~52, 61~67),DATA
peak to peak level:5V

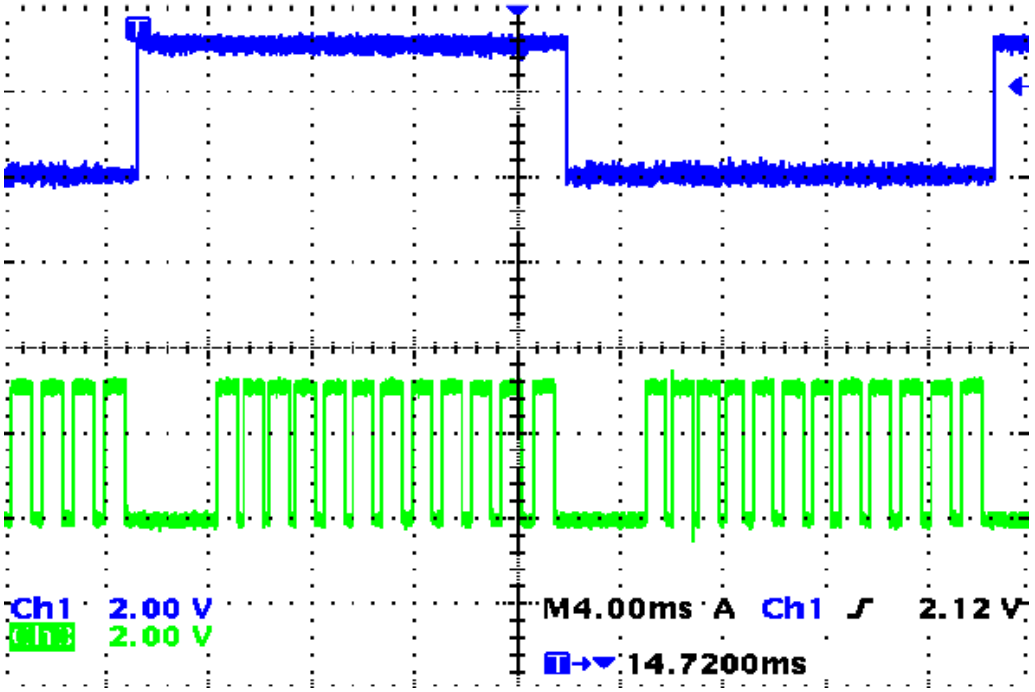
3



signal for trigger
(TP13)
peak to peak
level:3.3V

EC1,EC2,EC3,FC4,
GC5,GC6,GC7(20,
34,58,72),STB
peak to peak
level:5V

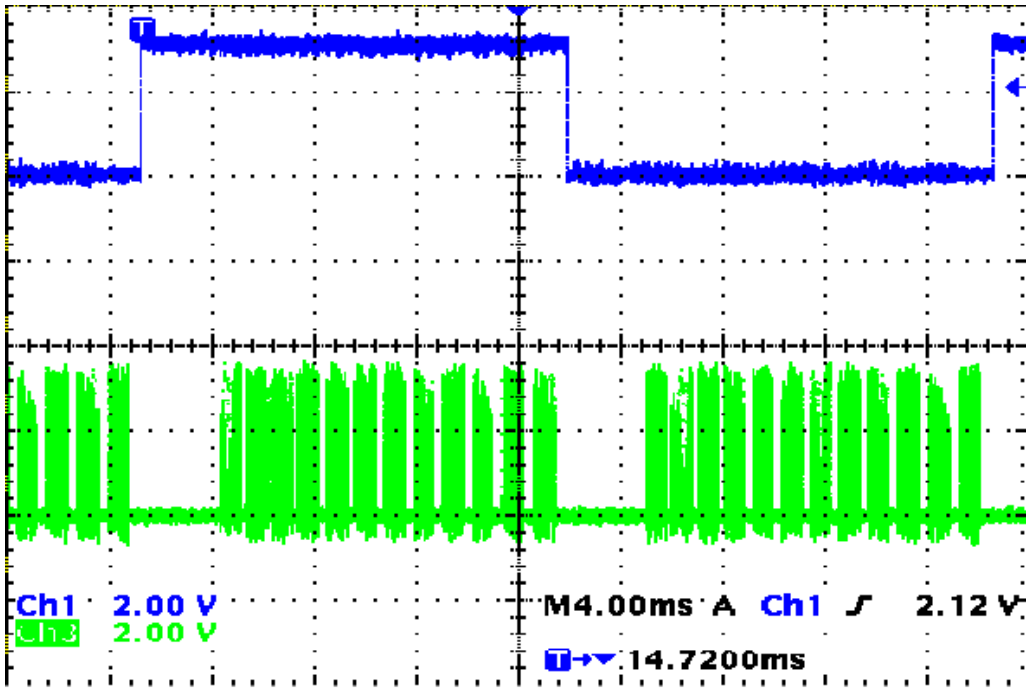
4



signal for trigger
(TP13)
peak to peak
level:3.3V

EC1,EC2,EC3,FC4,
GC5,GC6,GC7(15,
29,53,67),BLK
peak to peak
level:5V

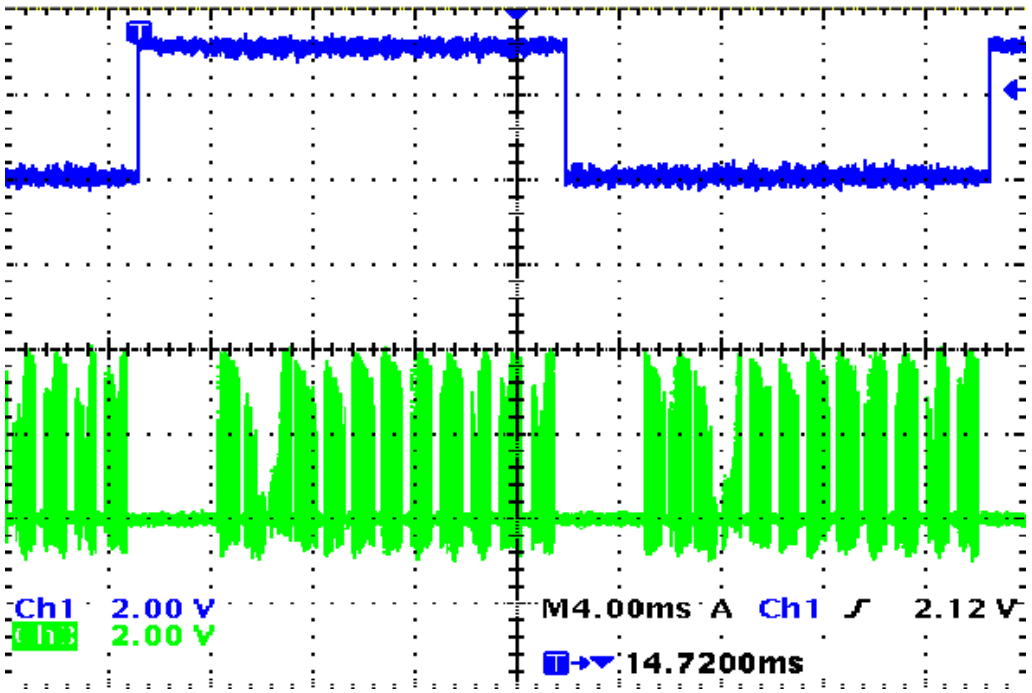
5



signal for trigger
(TP13)
peak to peak
level:3.3V

EC,EC2,EC3,FC4,
GC5,GC6,GC7(19,
57),SCLK_1
peak to peak
level:5V
Frequency:20MHz

6



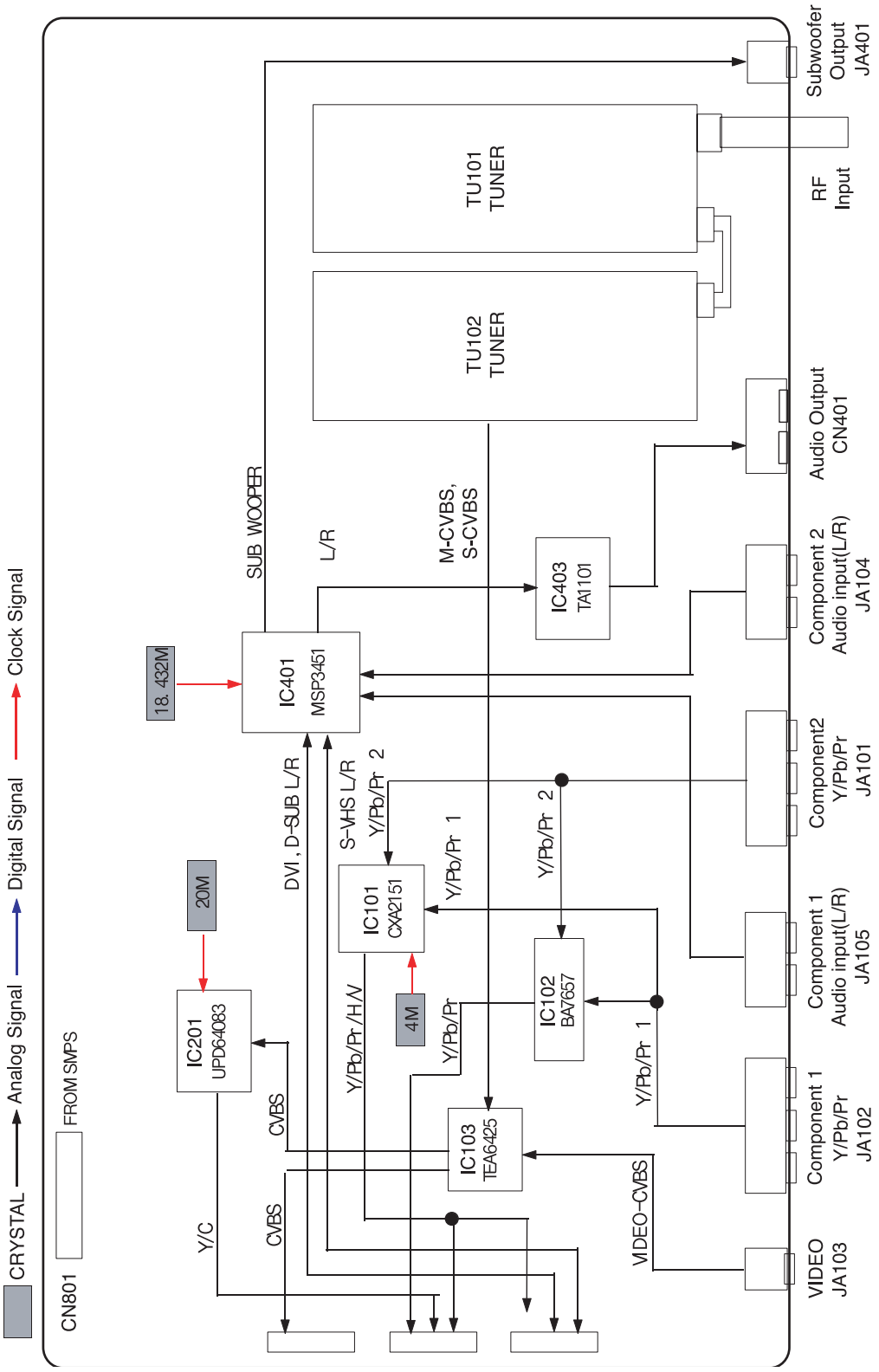
signal for trigger
(TP13)
peak to peak
level:3.3V

EC1,EC2,EC3,FC4,
GC5,GC6,GC7(33,
72),SCLK_2
peak to peak
level:5V
Frequency:20MHz

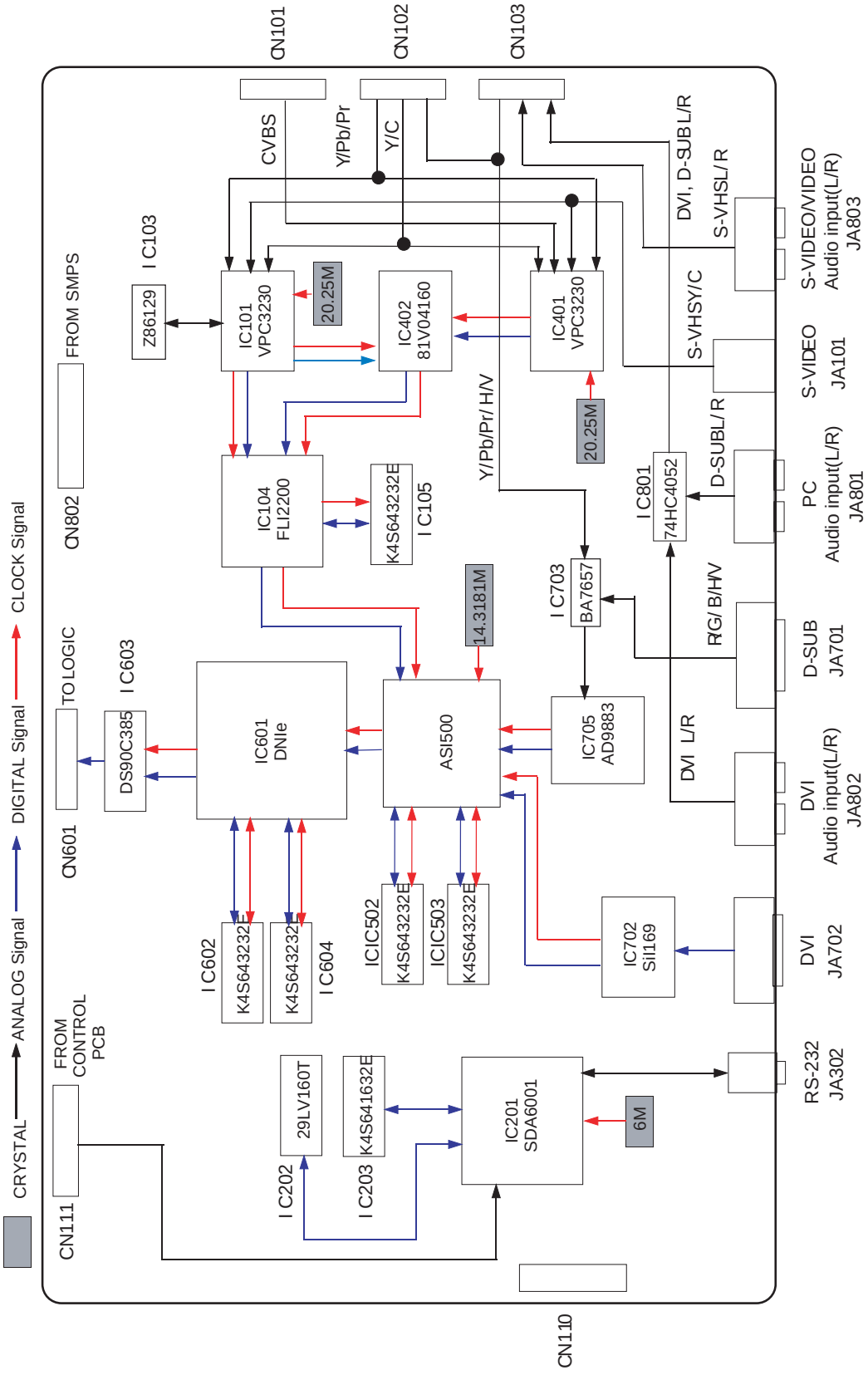
5-6 Video Circuit Part

5-6-1 Block Diagram

5-6-1(A) Analog Board IC & Signal Block Diagram



5-6-1(B) Digital Board IC & Signal Block Diagram



5-6-2 Inspections on Major ICs

1. SDA6001 (IC201) - MICOM

(1) Check whether the proper power is supplied. (3.3v, 2.5V)
(2) Check whether the No.73 Reset pin's output is High.
(3) Check I2C-BUS (I2C 1 : pins 98 and 99, I2C 2 : pins 100 and 101).
(4) Check whether the inputs/outputs between SDA6001 and MEMORY (IC203, IC205) are normal.
(5) Check whether the 6-MHz clock is connected to pins 108 and 109.

2. VPC3230 (IC101, IC401) ▶ Check when the input mode is set for TV, S-Video, Component1, or 2 (SD-level)

(1) Check whether the proper power is supplied. (3.3V, 2.5V)
(2) Check whether the No.15 Reset pin's output is High.
(3) Check I2C-BUS (pin 13 and 14).
(4) Check whether the output clock of LLC1 (pin 28) is 13.5MHz.
(5) Check the output on H SYNC (pin 56) andV SYNC (pin 57).
(6) Check the digital data outputs.

3. 81V04160 (IC402) ▶ Check the PIP operations when the input mode is for TV, S-Video, Component1, or 2 (SD-level)

(1) Check whether the proper power is supplied. (3.3V)
(2) Check the digital data inputs and outputs.

4. FLI2200 (IC104) - DEINTERLACER ▶ Check when the input mode is for TV, S-Video, Component 1, or 2 (SD-level)

(1) Check whether the proper power is supplied. (3.3V, 2.5V)
(2) Check wheter the No.48 Reset pin's output is High.
(3) Check I2C-BUS (pins 47 and 48).
(4) Check whether the data inputs are normal.
VPC_CLK (pin 40) : 13.5 MHz, VPC_HSYNC (pin 3) : 15.75 KHz, VPC_VSYNC (pin 4) : 60Hz
(5) Check whether the data outputs are normal.
FLI_CLK (pin 117) : 27 MHz, FLI_HSYNC (pin 92) : 31.5 KHz, VPC_VSYNC (pin 91) : 60Hz
(6) Check whether the inputs and outputs between FLI2200 and MEMORY (IC105) are normal.

5. CXA2151Q (ANALOG BOARD IC101) - COMPONENT S/W & SYNC SEPARATION ▶ Check when the input mode is for Component 1, or 2 (HD-level), and PC.

(1) Check whether the proper power is supplied. (5V)
(2) Check I2C-BUS (pins 56 and 57).
(3) Check whether the video input signals (pins 43, 48, 54) and the H (pin 30) and V (pin 31) input signals are normal.
(4) Check whether the data outputs are normal.
Y, Pb, Pr (pins 25, 26, 27), COMP_H (pin 22) : 45 KHz (for 720p), COMP_V (pin 23) : 60Hz

6. AD9883 (IC705) - A/D CONVERTER ▶ Check when the input mode is for Component 1 or 2 (HD-level) and PC.

(1) Check whether the proper power is supplied. (3.3V)
(2) Check I2C-BUS (pins 56 and 57).
(3) Check whether the video input signals (pins 43, 48, 54) and the H (pin 30) and V (pin 31) input signals are normal.
(4) Check whether the data outputs are normal.
R, G, B digital data outputs (RW708~RW713), ASI_SUB_H (pin 66) : 45KHz (for 720P), ASI_SUB_V (pin 64) : 60Hz, ASI_SUB_CLK (pin 67)

7. SII169CT100 (IC702) - TMDS RECEIVER ▶ Check the when the input mode is for DVI.

(1) Check whether the proper power is supplied. (3.3V)
(2) Check whether the power down pin's (pin 2) output is High.
(3) Check whether the DVI inputs are normal.
(4) Check whether the data outputs are normal.
R, G, B digital data outputs (RW701~RW706), DVI_HSYND (pin 48), DVI_VSYNC (pin 47), DVI_CLK (pin 44), DVI_DE (pin 46)

8. ASI500 (IC501) - SCALER

(1) Check whether the proper power is supplied. (3.3V, 2.5V) - Since it is BGA IC, measure the R or C parts on the power terminals.
(2) Check whether the inputs and outputs between ASI500 and MEMORY (IC502, IC503) are normal.
(3) Check whether the outputs of FLI2200, AD9883, and SII169CT100 are input into ASI500 are normal.
(4) Check whether the data outputs are normal.
R,G,B digital data outputs (RW501~RW506), MN_IN_H (RW507), MN_IN_V (RW507), MIN_IN_CLK (RW507)

9. DNIe (IC601) - PICTURE ENHANCER

(1) Check whether the proper power is supplied. (3.3V, 2.5V)
(2) Check whether the Reset pin's output is High. (pin 74)
(3) Check I2C-BUS (pins 1 and 2)
(4) Check whether te outputs of ASI500 are input into DNIe normally.
(Digital R, G, B and HSYNC, VSYMC, CLK)
(5) Check whether the data outputs are normal.
R, G, B digital data outputs (RW602~RW607), OUT_HSYNC (pin 10), OUT_VSYNC (pin 9), OUT_CLK (pin 12)

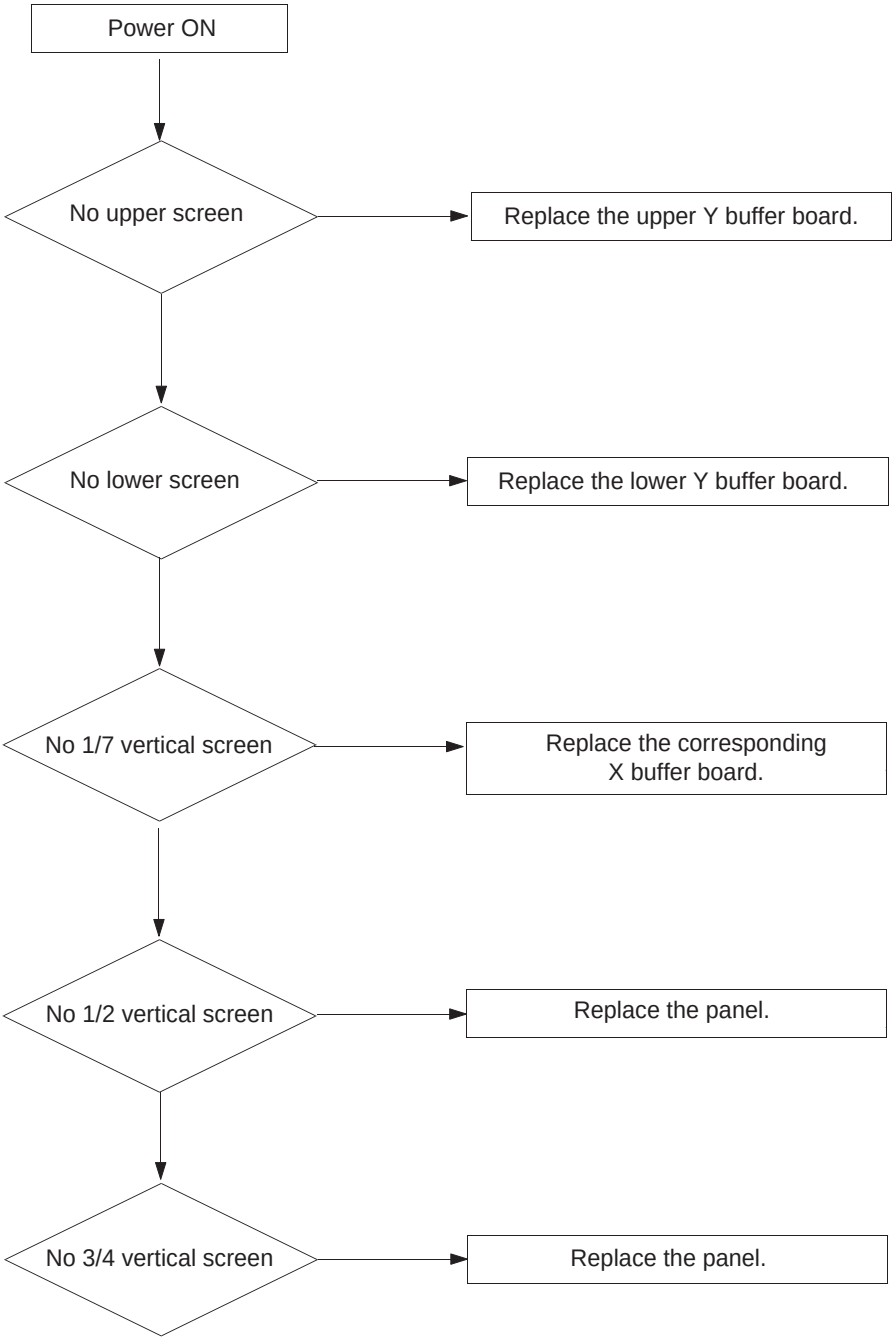
10. DS90C385 (IC603) - LVDS TRANSMITTER

(1) Check whether the proper power is supplied. (3.3V)
(2) Check wether the power down pin's (pin 32) output is High.
(3) Check whether the outputs of DNIe are input into DS90C385 normally.
(4) Check whether the LVDS data outputs are normal.

6. Troubleshooting

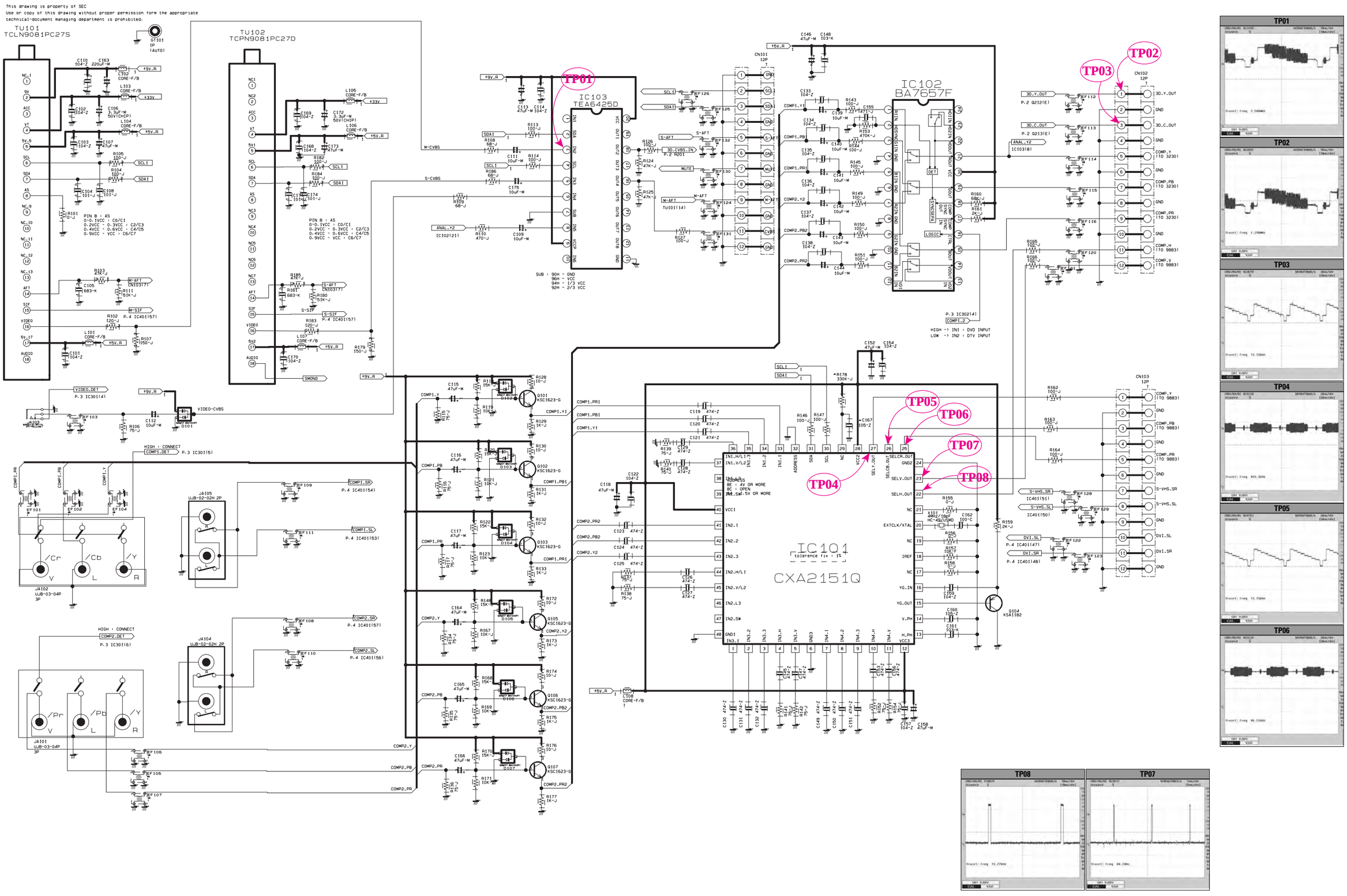
6-1 Entirely no screen (Main Body)

6-2 Partly no screen (Main Body)



7. Schematic Diagrams

7-1 ANALOG-1



7-2 ANALOG-2

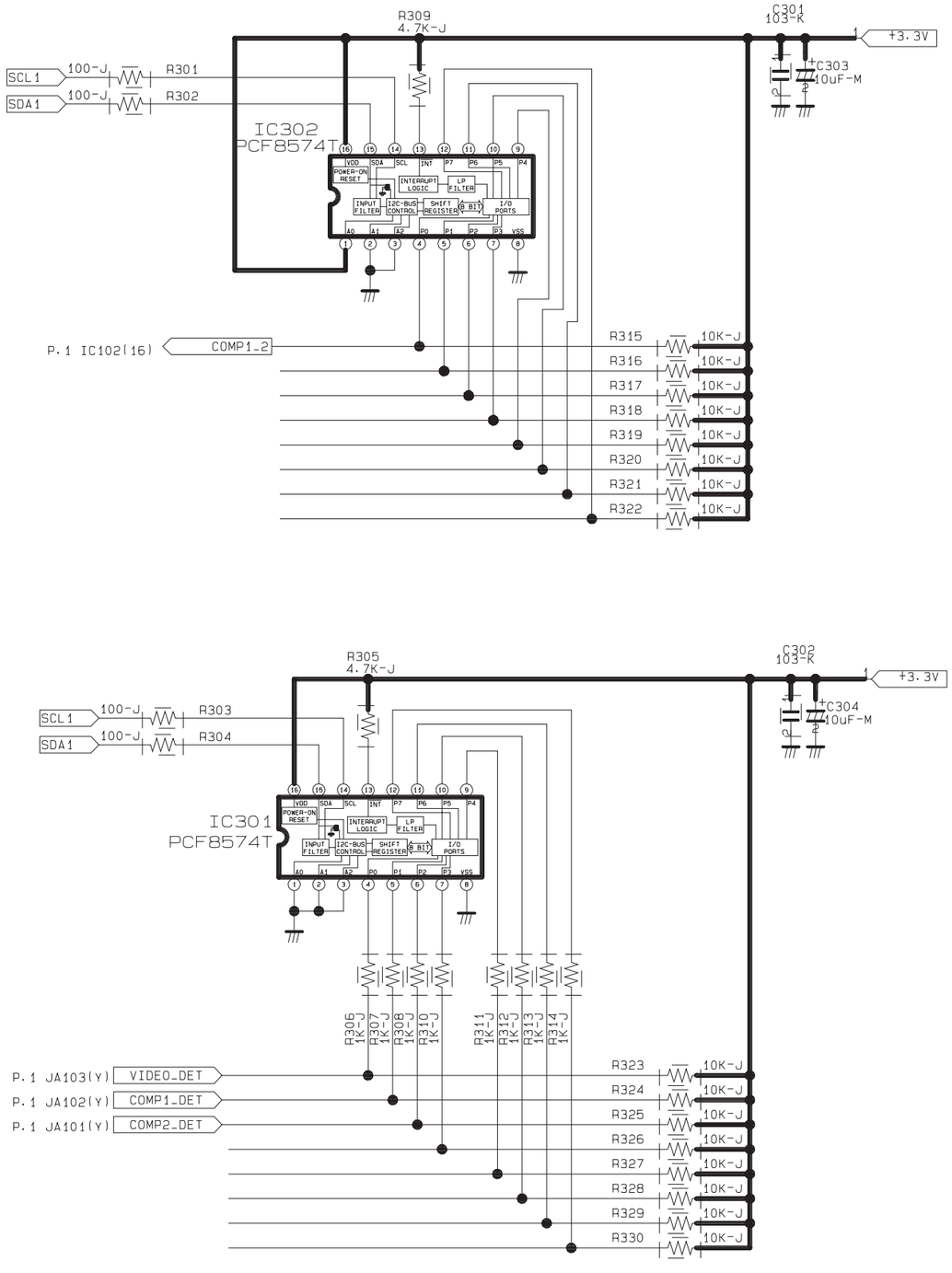
IC201
UPD640836F
12189

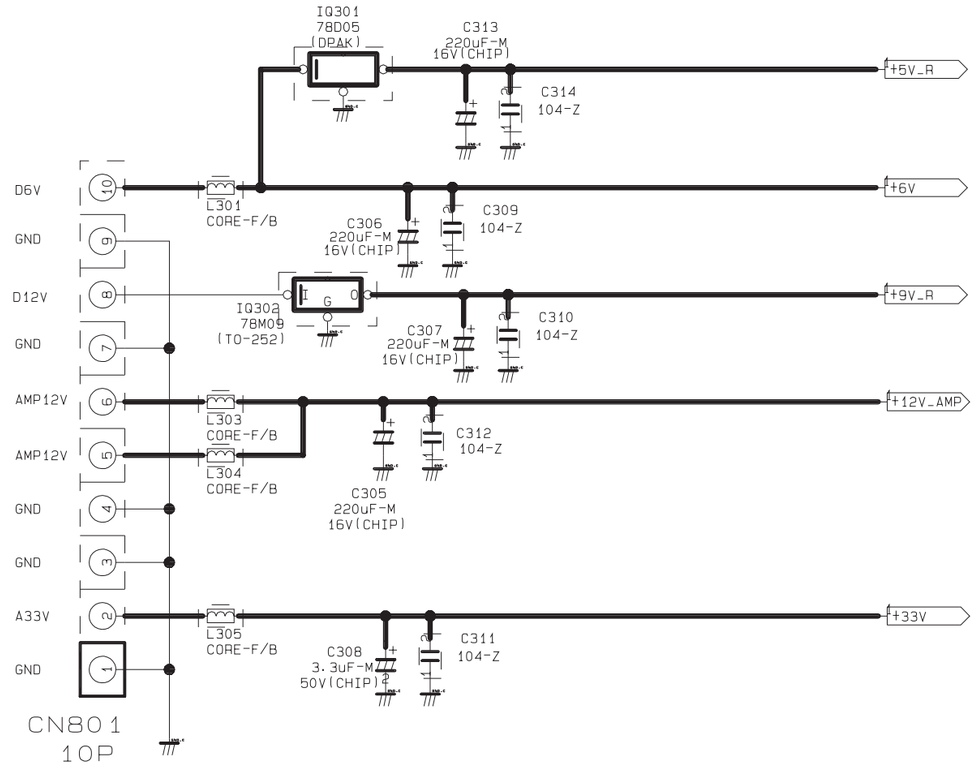
UPD64083

COMPOSITE_SYNC_SEPARATION

POLARITY_CHECK

7-3 ANALOG-3





PCB DRAW : CAUTION : HEIGHT 2.8 ABOVE
TEXT : HEIGHT 1.6

CAUTION : Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type.

7-4 ANALOG-4

IC401
MSP3451G
(QFP)

IC402
TL062CDT

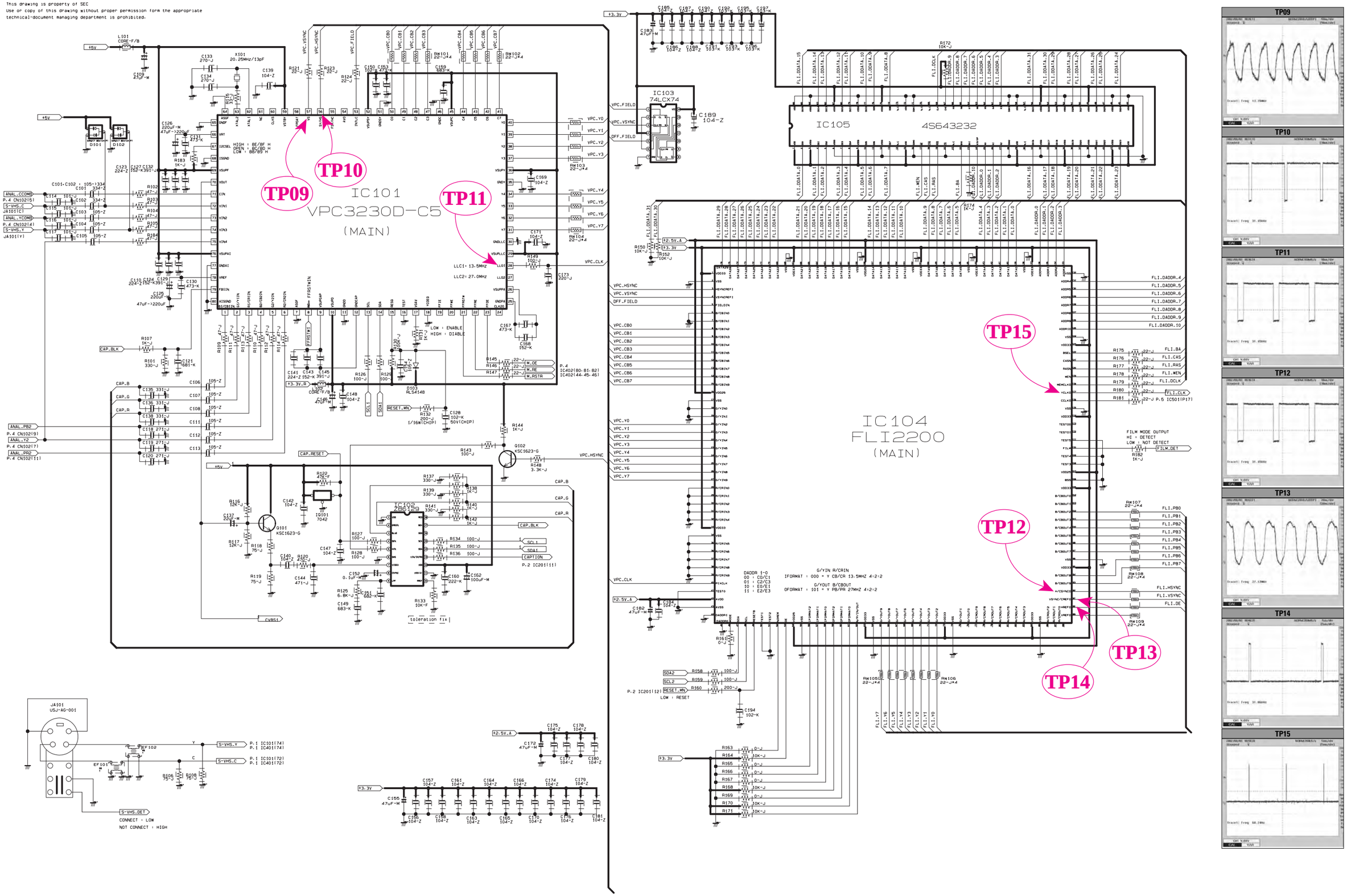
IC403
1101

IC404
TL062CDT

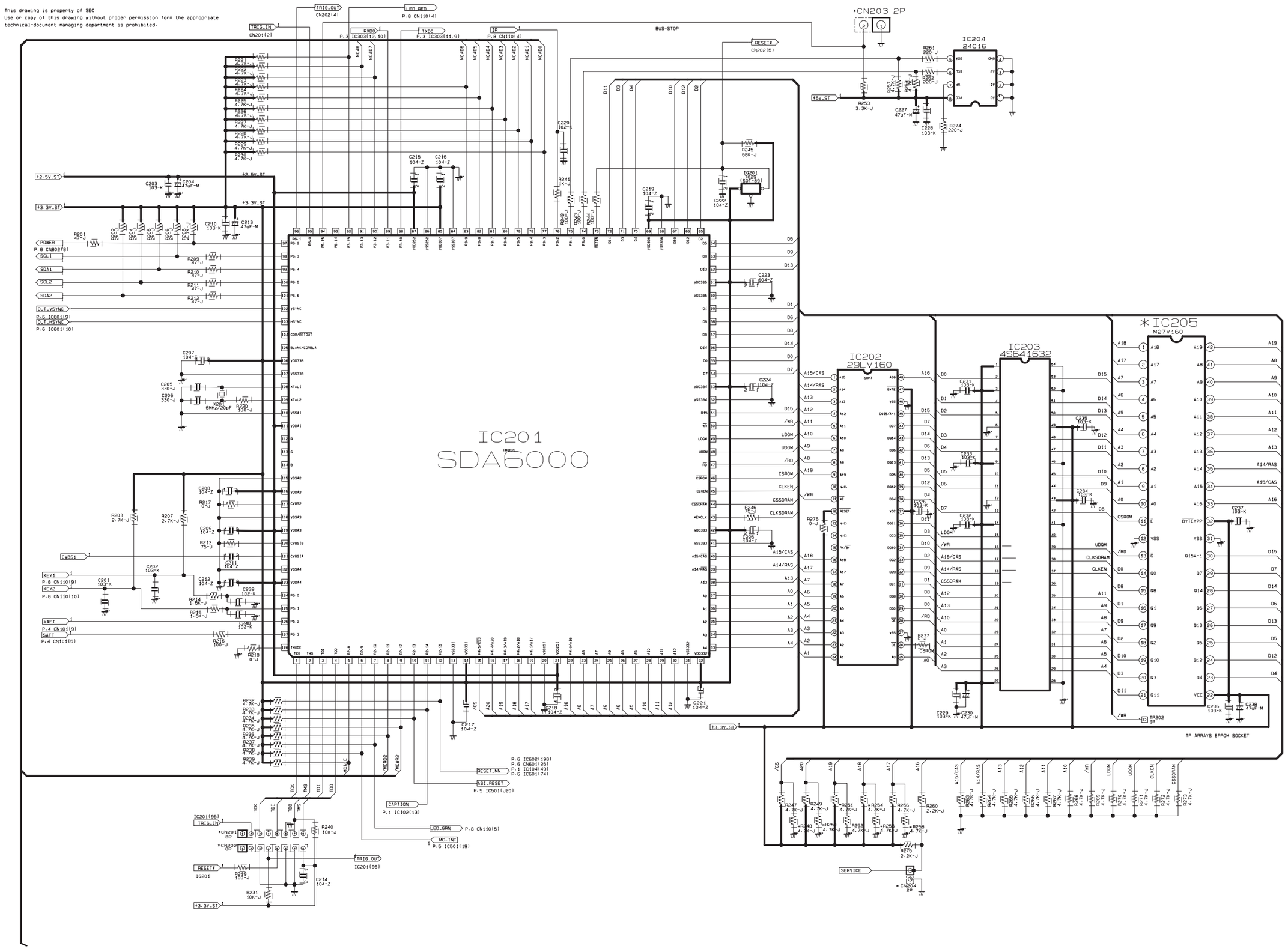
MUTE

SOUND OUTPUT - JACK VIEW
R- R+ L- L+

7-5 DIGITAL-1



7-6 DIGITAL-2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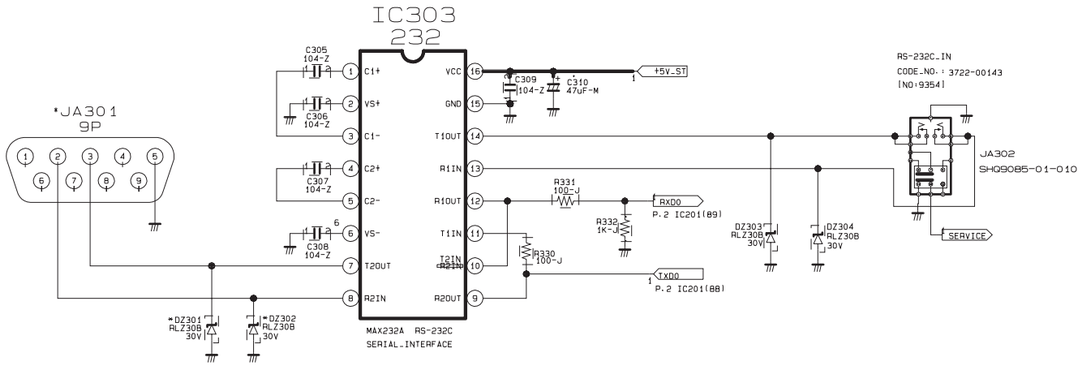
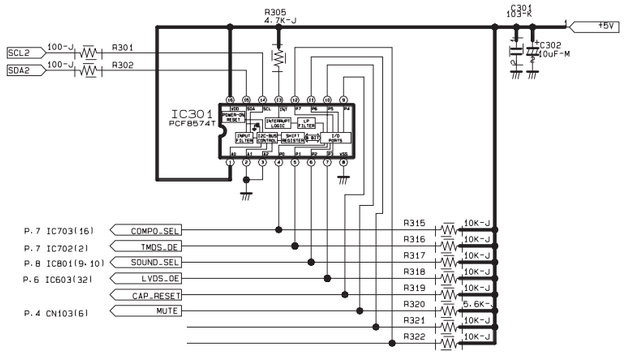
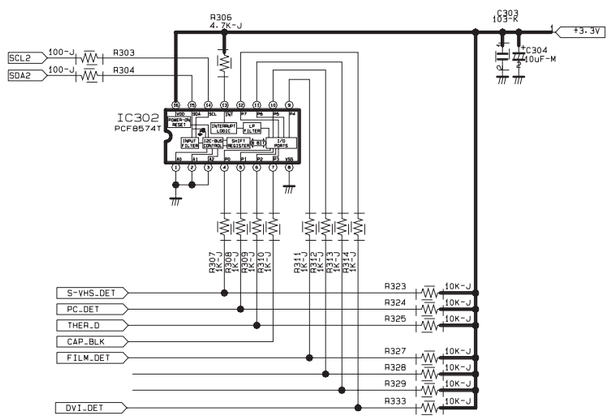
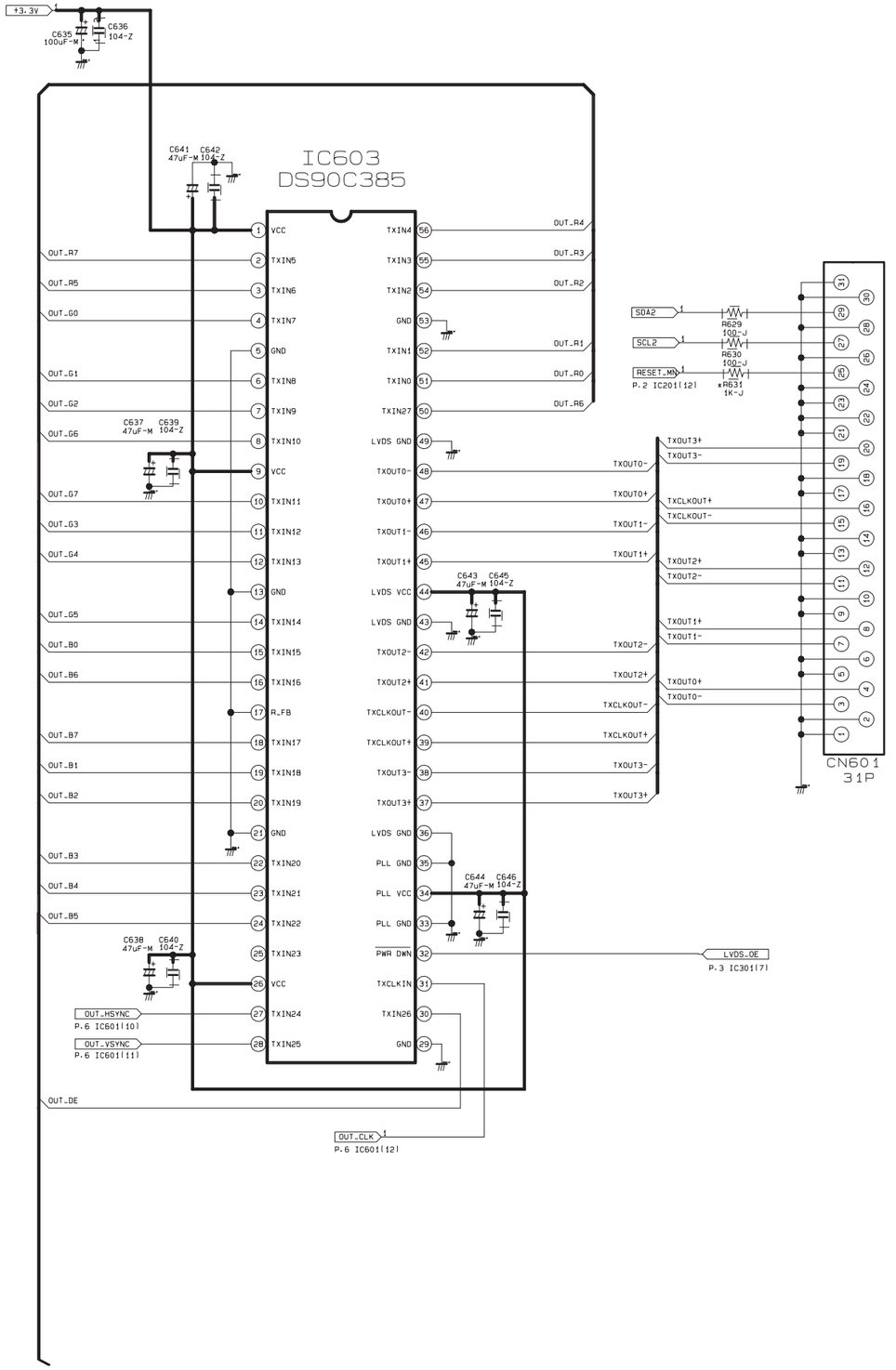
technical-document managing department is prohibited.
IC201
SDA6000
IC202
29LV160
IC203
4S641632
IC204
24C16
IC205
M27V160
CN203 2P
CN204 2P
IQ201
7029
IQ201
SERVICE
TP ARRAYS EPROM SOCKET
BUS-STOP
TRIG.OUT
LED_RED
TRIG_IN
RXD0
TXD0
IR
RESET#
+5V_ST
+2.5V_ST
+3.3V_ST
POWER
SCL1
SDA1
SCL2
SDA2
OUT_VSYNC
OUT_HSYNC
CVBS1
KEY1
KEY2
MAFT
SAFT
RESET_MN
ASI_RESET
CAPTION
LED_GRN
MC_INT
TRIG_OUT

7-7 DIGITAL-3

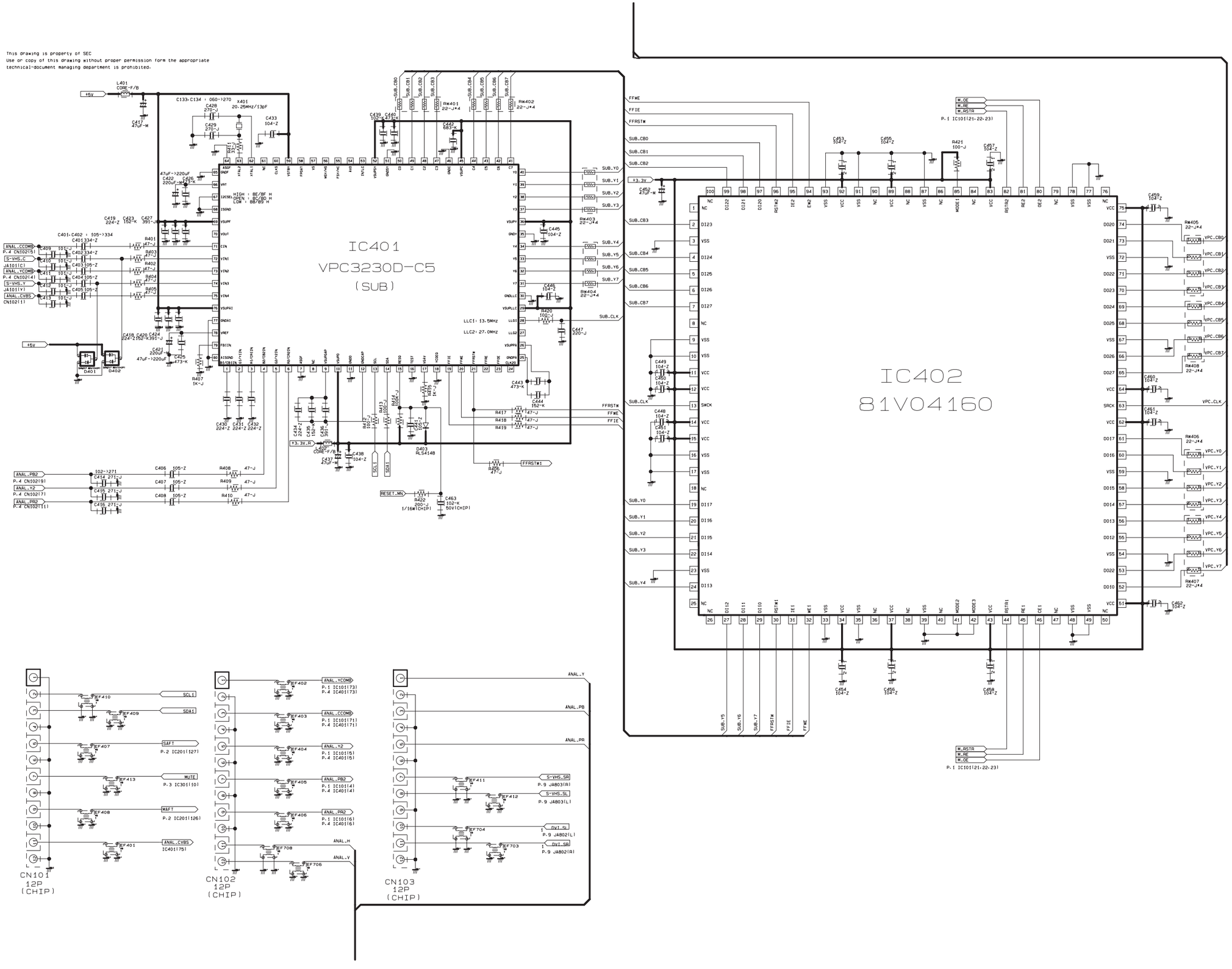








7-8 DIGITAL-4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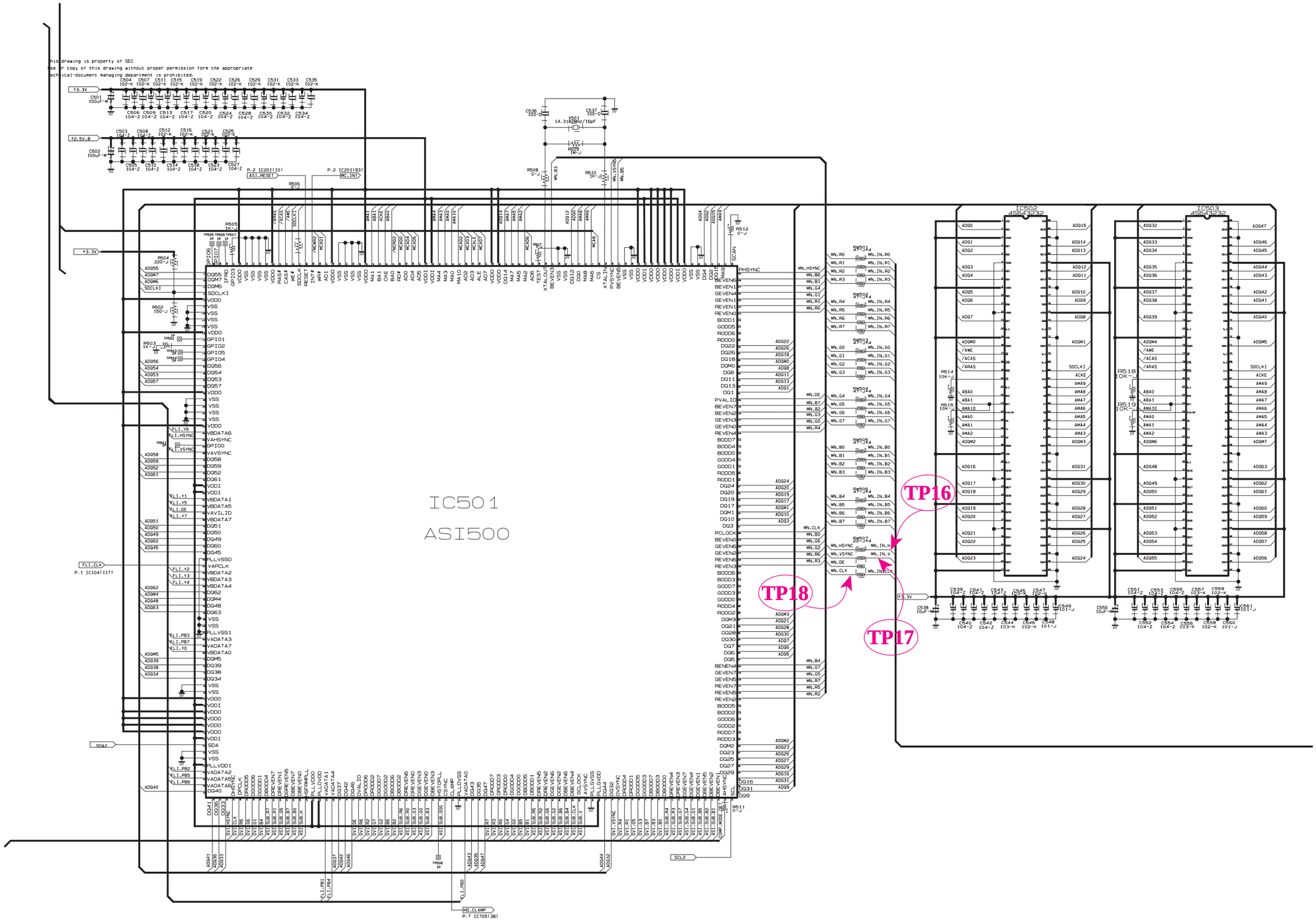
IC401
VPC3230D-C5
(SUB)
IC402
81V04160
CN101
12P
(CHIP)
CN102
12P
(CHIP)
CN103
12P
(CHIP)

7-9 DIGITAL-5



7-10 DIGITAL-6

IC601

DNIe

TP19

TP20

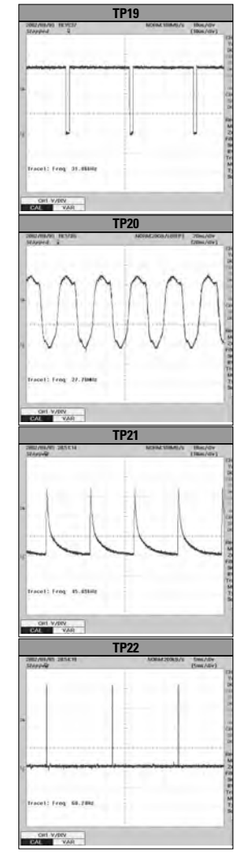
TP21

TP22

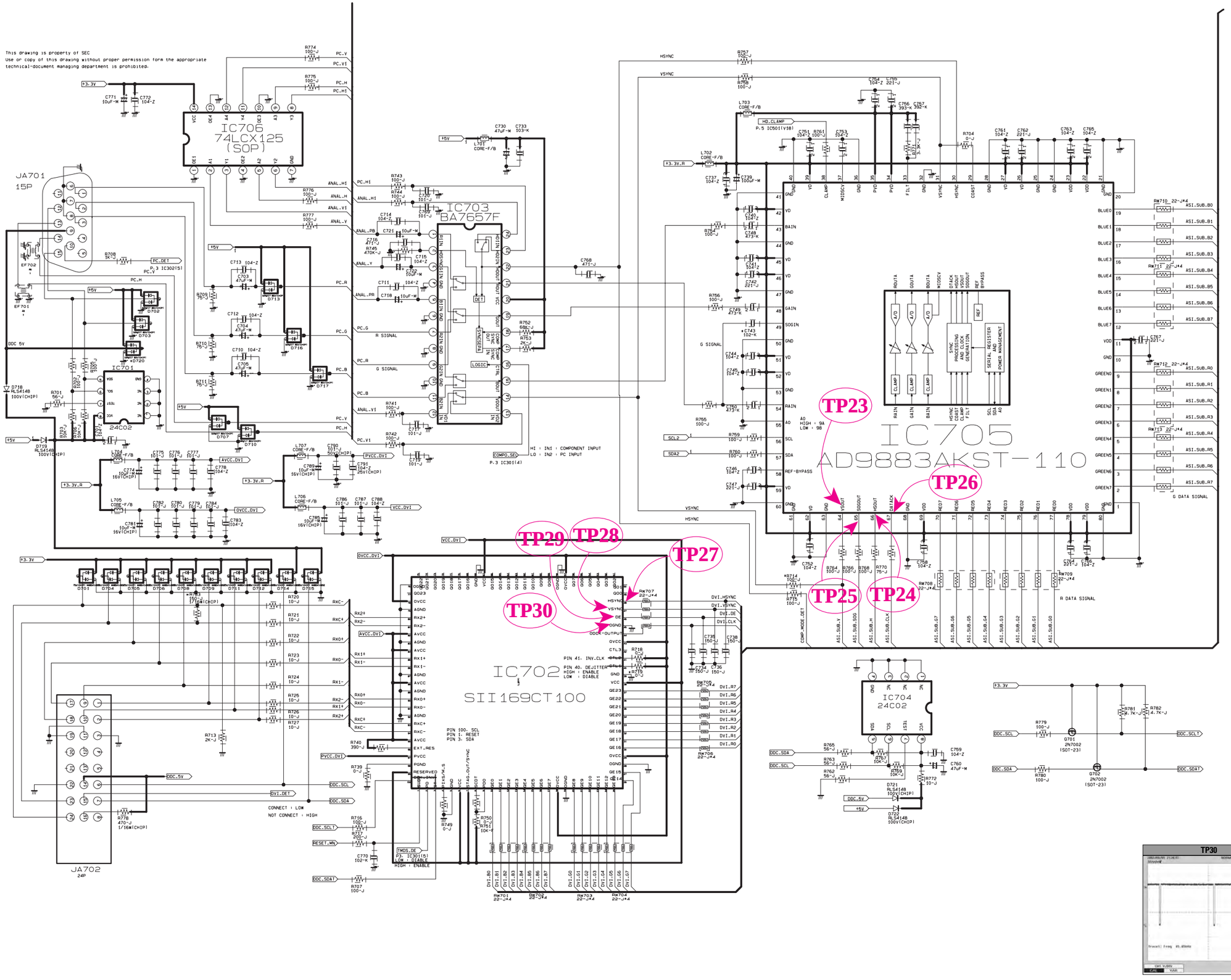
ADDR1-0
00 : CB/C9
01 : CA/CB
10 : CC/CD
11 : CE/CF

IC602 4SE43232

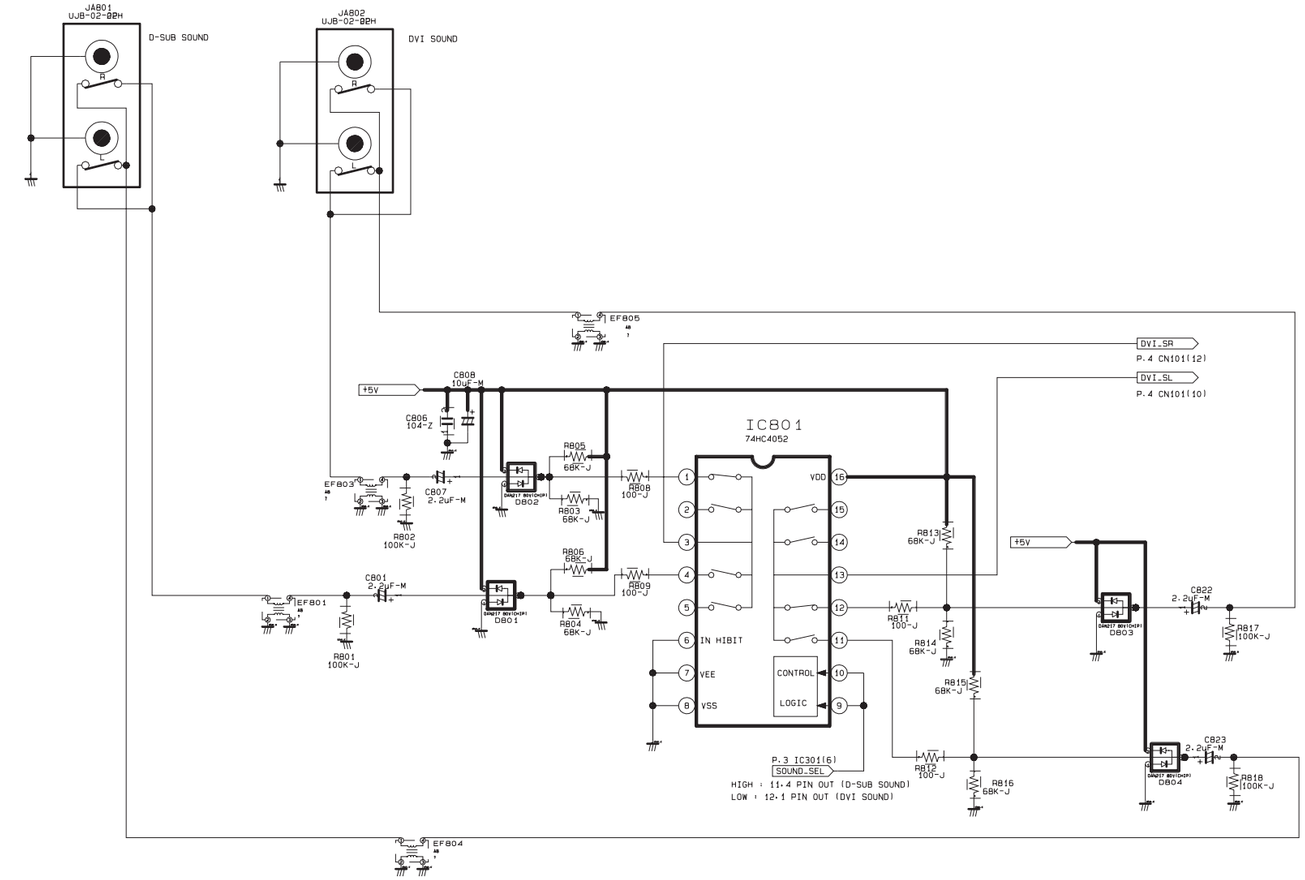
IC604 4SE43232

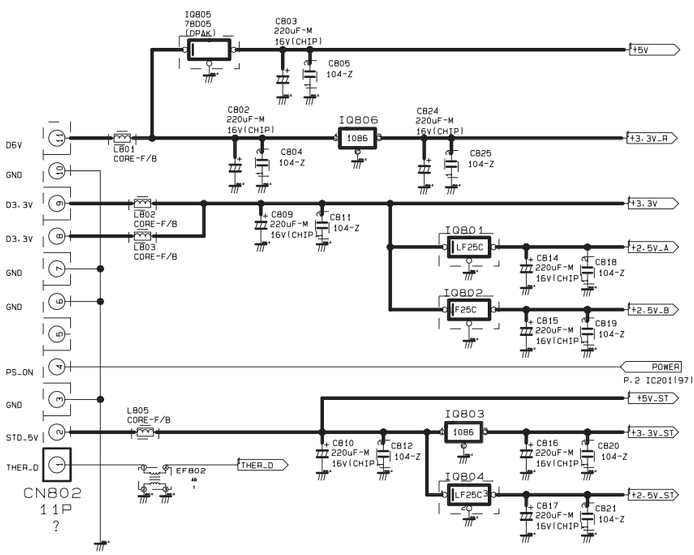


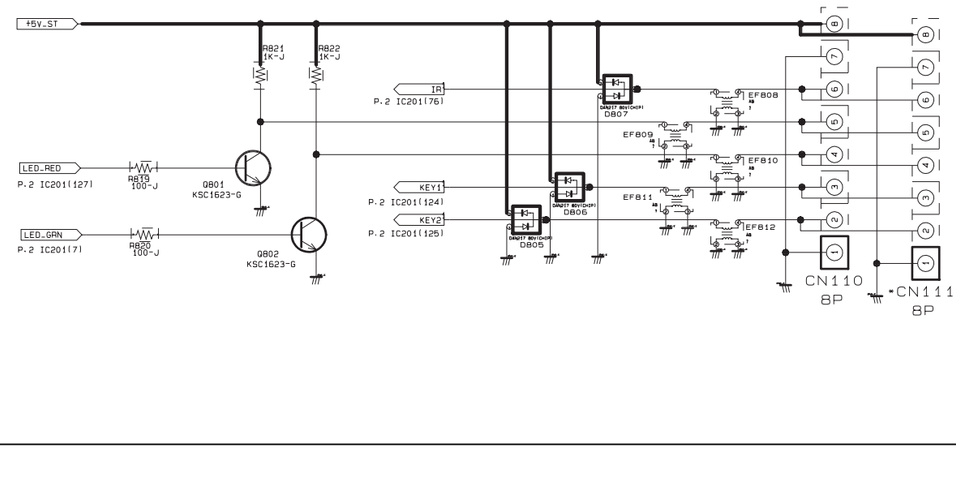
7-11 DIGITAL-7



7-12 DIGITAL-8







7-13 CONTROL